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CONTENTS

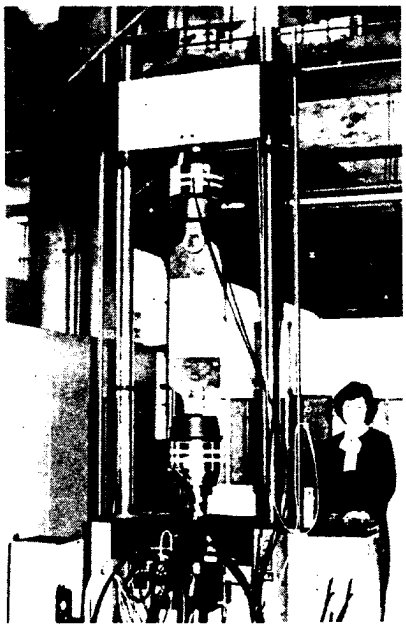
SUPERCONDUCTIVITY

National Aerospace Laboratory (NAL) News

43062088 Tokyo KOGIKEN NYUSU in Japanese Apr 89 pp 1-10

[Text] MTS-500KN-Fatigue Tester

In 1988, a vertical, hydraulic fatigue tester with a 500 KN loading capacity was installed in the Structural Dynamics No 1 Building in an effort to update the composite material structural test facilities. This device is also expected to replace the resonance-type Schenck PB 30 Fatigue Tester (Capacity: 30 tons) which was installed about 30 years ago, and is no longer capable of full-scale performance due to decrepitude.



Photograph 1. Crack Propagation Test with MTS-500-KN Fatigue Tester

Photograph 1 illustrates a fatigue test being performed on an aluminum alloy plate with this device. The tester can be controlled by the function generator on the control panel as well as via a computer to perform a variety of strength evaluation tests.

Listed below are the principal capabilities and the basic test conditions when performed by a control panel input.

Maximum Compression/Tension Force	± 500 KN
Maximum Displacement	± 75 mm
Loading Rate	0 to 10 Hz (Displacement: 3 mm)
Load Wave Shape	Sine wave, triangular wave, and rectangular wave
Hydraulic Source Discharge	235 l/min
Hydraulic Discharge Pressure	21 MPa
Hydraulic Chuck	(Standard mount)
Control Mode	Displacement, load, stress control
Maximum Distance between Chucks	(When hydraulic chucks are used) 1,350 mm
Interframe Distance	762 mm

Major tests that can be performed with the computer control using the standard software are:

* Static load stretch and compression tests (can be automatically switched to displacement control after maximum load is reached)

* Low cycle fatigue tests (constant amplitude load: up to maximum of two Hz)

* Breakage toughness tests

  By using a specified compact test piece and an extensometer, a breakage toughness value per the ASTM specifications is given promptly.

* Random flight load tests

  By setting up and carrying out missions in a tournament fashion as shown in Figure 1, random load tests can be performed. A load can be given with a pre-determined frequency or rate of change at the time of hydraulic supply. In the case of a random load test involving large and small loads, a smooth load wave shape with little errors can be obtained by controlling the change rate of smaller loads.

In the future, in order to be able to use this fatigue tester to perform strength evaluation tests on aerospace composite material structures under actual use conditions, we are trying to complete an environmental simulation device as described below.

(1) Temperature-humidity controlled environmental cabinet

Temperature range: -50 °C to 150 °C
Humidity range: 30 to 95 percent (relative humidity)
Temperature change rate: 4 °C/min (maximum)
(Any environmental cycle can be programmed.)

(2) High temperature strength evaluation environmental cabinet

Temperature: room temperature to 350 °C
Temperature change rate: 5 °C/min

(3) High frequency heated test device for superhigh temperature tests

Temperature: 100 °C to 1,700 °C
Temperature change rate: >50 °C/min
Sample: round rod and plate (conductors only)

We hope to be able to cope with the domestic and overseas needs for the diversified aerospace structure development by using the tester incorporating these environmental test devices. (Hiroyuki Terada, Structural Dynamics Department).

Use Environment of GCP at NAL

Recently, much larger-scale computations and much more complicated computations than previously possible have become a reality due to the improvement in computer capabilities and the advancement of the numerical simulation technology to master the computer. As a result, the visualization technology has become indispensable as a verification method for computation results, and the demand for graphic and image control is rapidly increasing. However, each manufacturer makes its own version of the drawing library for the use of a graphic controller, forcing the user of a particular graphic controller to learn the corresponding library's functions to formulate a drawing program.

To improve this situation to offer an efficient graphic control environment to the user so he can formulate a drawing program regardless of the make of his device, it was necessary to develop a graphic control package that can be commonly used with any graphic controller. Thus, in FY85, the National Aerospace Laboratory (NAL) initiated the development of its own graphic control package (GCP). This GCP is not only a graphic control package that can be commonly used with any graphic controller but also can function as an application drawing programmer and a three-dimensional graphic data display for the grid diagrams, contour maps and oil flow diagrams, which are particularly in high demand at NAL.

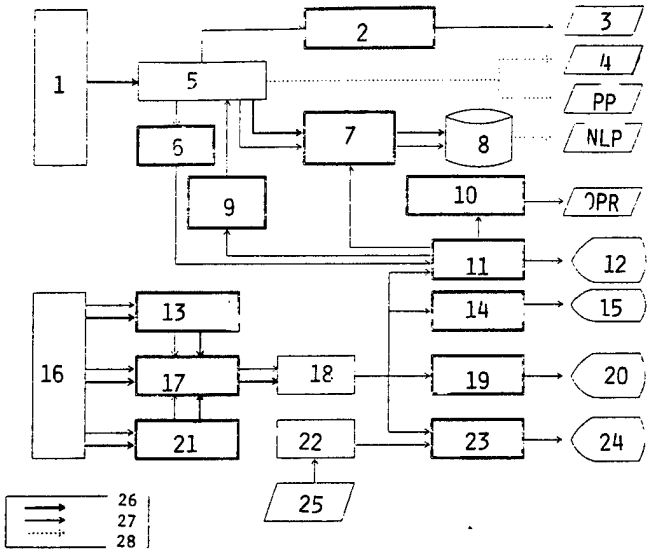
The GCP was also incorporated in the numerical simulator system (called NS system) at the time of its installation, and the system began operating in February 1987. Thus, the use environment of graphic software has been offered to users, including those who are not familiar with graphic control. Thus, they can perform with relative ease operations from drawing programming to graphic output without relying on a particular graphic controller.

Shown in the attached diagram is the graphic control flow actually run with the NS system. The entries in the double squares in the diagram, denote the GCP programs. In the batch control, a user can select any one of XY-plotter (XY), printer-plotter (PP) or Japanese language line printer (NLP), as the output device for graphic results of a drawing program described by the Calcomp Library. These graphic data can be monitored by a two-dimensional GD prior to the output by a selected device. At that time, by preparing various conversion programs that can be used at a command level, the user can not only cancel the output or change the output device but can also easily access to an XY, PP, NLP or office printer (OPR) for outputting even enlarged or rotated graphics.

In the TSS control, a user can display graphics by any one of TSS/GD, two-dimensional GD, three-dimensional GD and image GD, as long as a drawing program described in the GCP library is used. Furthermore, because GCP includes the Calcomp library functions, a drawing program for the batch control can be used in the TSS control.

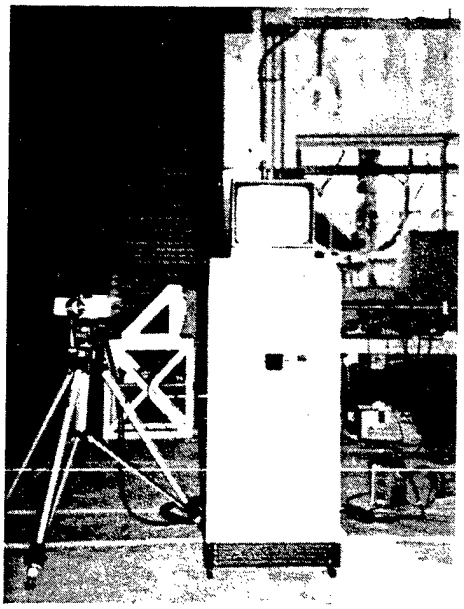
GCP, with the availability of a display program to match a display device, realizes the independence of such a drawing program from the device. Thus, the GCP user can easily switch display programs by command to suit a display device. In addition, display programs of GCP are designed so that the functions unique to a device (for example, the hidden lines and planes control functions for displays with an image GD) can be made automatically available. Additional software is available for the realization of three-dimensional graphic data displays and local control functions (functions to rotate, move, enlarge or reduce display graphics) for two-dimensional graphic displays and image displays. Especially for the multiple installation of the two-dimensional graphic displays, graphic outputs can be directed to any one of XY, PP, NLP and OPR, by any one of various conversion programs similar to the monitor control.

GRAPHIC CONTROL FLOW IN NS SYSTEM



(1) Calcomp-format drawing program
(2) Format change program for open XY
(3) XY (open)
(4) XY (closed)
(5) Calcomp-format interim data
(6) New monitor program
(7) Format change program for NLP output
(8) Spool file
(9) Format change program for XY output
(10) Format change program for OPR output
(11) Program for two-dimensional display
(12) TSS/GD two-dimensional GD
(13) Simulation Calcomp program
(14) Program for three-dimensional display
(15) Three-Dimensional GD
(16) GCP-format drawing program
(17) GCP basic program
(18) GCP-format graphic data
(19) Program for NEXUS display
(20) Image GD NEXUS
(21) GCP application program
(22) Image data
(23) Program for FIVIS display
(24) Image GD FIVIS
(25) Image scanner
(26) Batch control
(27) TSS control
(28) Others

Another environment is also available to automatically create animated graphics from static graphics in display as described above by the use of a software shutter. (Kazuyo Suematsu, Mathematical Analysis Department)



(1) Figure 1. High-speed Video Analyzing System

Table 1. Specifications of High-speed Video Analyzing System

Filming Speed:	60 to 2,000 frames per second (maximum 12,000 frames per second when a frame is divided into six)
Resolution Capability:	192 x 240 pixels
Recording Time:	45 seconds to 25 minutes
Reproduction Speed:	60 frames per second
Output Interface:	GP-IB
Dimensions:	50 x 50 x 100 cm
Weight:	Approximately 120 kg

The high-speed video analyzing system (maximum filming speed: 12,000 frames per second), which was acquired by the FY87 revised budget, has been used for impact tests, wind tunnel tests and combustion tests of composite materials after the completion of adjustment and control programs. This device has been used for impact tests of new materials and research concerning phenomena of superhigh speed and combustion in R&D of revolutionary aircraft propulsive engines including air-breathing engines. An outside view of this device is shown in Figure 1. It consists of a main unit and a camera, and the specifications are given in TAble 1. This device has a poorer resolution (192 x 240 pixels) than previous high-speed photographic devices, but has advantages of enabling long-hour filming and instant low-speed replays and observations. In particular, because the contents of the built-in image buffer memory (64 patterns per pixel) can be stored for each frame in a computer via the GP-IB interface, the screen can be quantitatively analyzed by an appropriate image control program; thus, potential applications of this device for many areas are imaginable. The establish-

ment of filming conditions, start and stop, and the index search of a tape can be controlled by a personal computer through the GP-IB interface.

Figure 2 illustrates the transformation process of a composite flat sheet (Kevler-carbon hybrid material) during an impact test. One can visualize, from the change in the surface reflection, the state of transformation at the moment of impact (t = 0) and the propagation of cracks to the carbon composite material at the surface. After 0.25 ms, a bullet (made of an ABS resin) is almost through the sheet, and the surface carbon layer is clearly being destroyed faster than the Kevler inner layer.

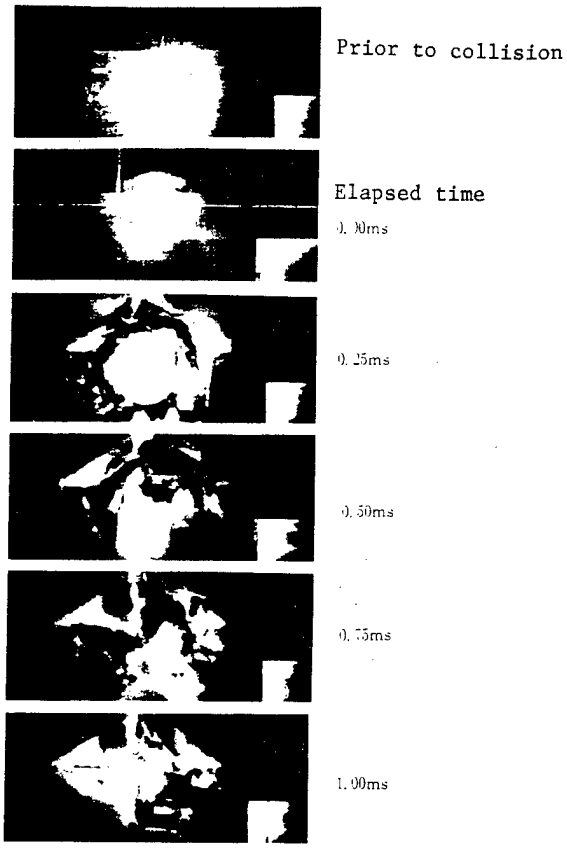


Figure 2. Kevler-Carbon Hybrid Material (0/90 layered)

Collision speed: 181.7 mm/sec
Filming speed: 4,000 frames/sec

The high-speed video camera is a powerful tool for studying actions in the super-high flow transition phenomenon and in the laser ignition phenomenon. Figures 3 and 4 show examples of laser-Schlieren images as observed by the camera. Figure 3 illustrates an example of a two-dimensional jet stream intersection perpendicularly with the main stream of Mach-two. One can observe the movement of shock waves accompanying the deceleration of the main stream caused by the jet stream's strong blocking and the change of peeling conditions near the wall. Figure 4 consists of continuous photographs (12,000 frames per second) showing the ignition of a methane-air thin mixture with YAG pulse laser. The photographs clearly show the generation of strong gas expansion waves after the breakdown and the subsequent formation of a flame nucleus.

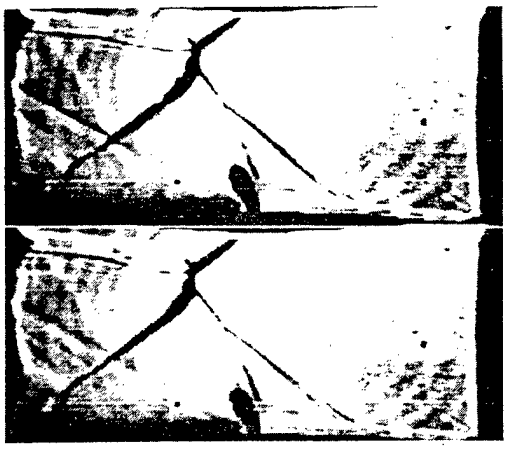


Figure 3. Interference by Supersonic Jet Stream

Filming speed: 4,000 frames/sec

Because of the excellent results obtained for the observation and measurement of high-speed phenomena, we plan to further improve the illumination method and develop an image control system to use this device for test research in many more areas. (Akinori Ogawa and Kunihisa Eguchi, Motor Department)

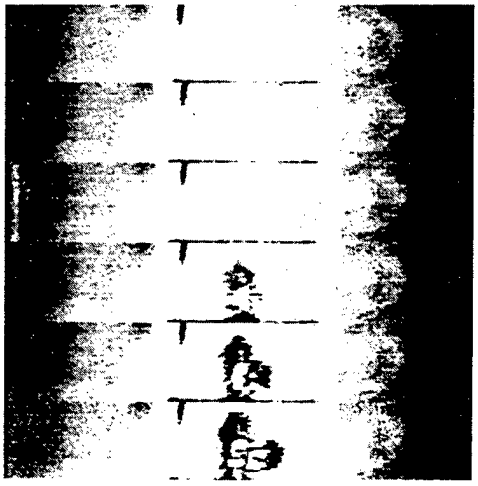


Figure 4. Laser Ignition of Methane/Air Mixture

Filming speed: 12,000 frames/sec

Wind Tunnel Experiments on Superhigh-speed Intake (Elemental Research on Air-Breathing Engine)

A study on the intake (air inlet) for high-speed planes has been conducted at NAL for the technology development concerning supersonic and ultrasupersonic planes as well as for the elemental research concerning turbo type air-breathing engines for space planes. The intake for high-speed planes is

an extremely important element of engine performance, because it performs efficient ram compressions and maintains required air flow volumes. However, not much research has been done on this subject in Japan, and Japan's own data have been meager. Thus, the Intake Research Association was inaugurated by NAL, Science University of Tokyo and Ishikawajima-Harima Heavy Industries Co., Ltd., to do test research concerning the intake. The Association's initial projects were literature survey and research method examination. As a result, the initial goal was selected as the acquisition of basic aerodynamic technology for the intake targeting the Mach-three class; the test research was started with emphasis on model testing using a supersonic wind tunnel.

The test to be discussed here is the most basic form of the supersonic wind tunnel test at Mach-three, using a fixed-shape intake model in conjunction with a three-shock system consisting of one external compression shock and two internal compression shocks. The specific aims of the test were: (1) to acquire basic technological data for the Mach-three class intake to fill information blanks in Japan, (2) to acquire key technologies, such as design/production and testing methods for the supersonic intake model, and (3) to gain technical guides for the purpose of improving the performance, speed and stable operation of the intake.

The model's outline is given in Figure 1. Its specifications are summarized in Table 1. The model has been designed to first generate oblique shock by a 15-o wedge, create the second oblique shock by receiving the first shock with a five or nine-degree cowl, and produce terminal shock by a throat set up in the vicinity of the spot where the second shock reaches the upper wall. The compression by the shock occurring upstream of the cowl is called external compression and the compression by the shock occurring downstreams of the cowl is called internal compression; thus, the compression is a mixture of the two. In this aerodynamic design, the theoretical compression recovery coefficient is 0.62 at most (with the five-degree cowl).

The model has an air-drawing hole at the upper wall situated upstream of the throat and an air-drawing valve to control the air drawing in order to secure the start-up of the intake and assure the stability of shocks. Inside the model, there is a movable flow plug to adjust the back pressure of the intake and cause the terminal shock in the throat. Both the flow plug and the air-drawing valve can be controlled from the outside.

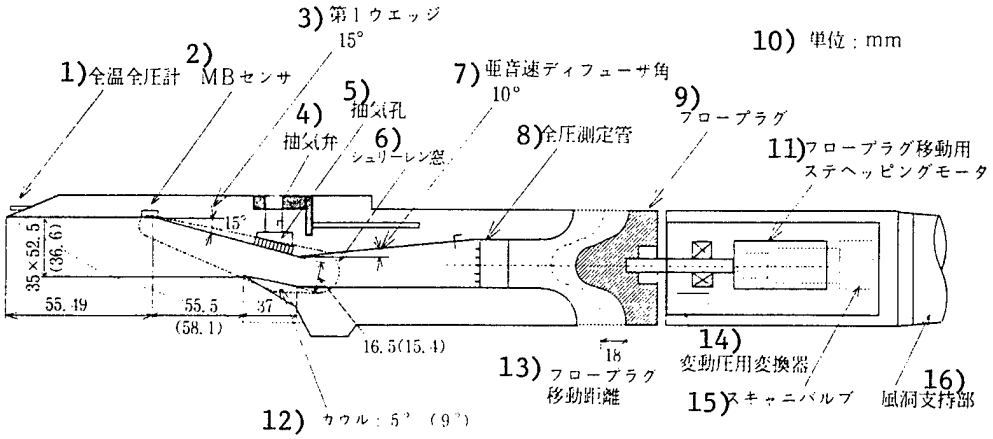


Figure 1. Outlines of Supersonic Intake Model

(1) Total temperature, total pressure gauges
(2) MB sensor
(3) First wedge
(4) Air intake valve
(5) Air intake inlet
(6) Schlieren window
(7) Subsonic diffuser, angle 10°
(8) Total pressure gauge pipe
(9) Flow plug
(10) Unit: mm
(11) (Stehepping) motor to move flow plug
(12) Cowl: 5° (9°)
(13) Flow plug displacement
(14) Variable dynamic pressure converter
(15) (Scanny) valve
(16) Wind tunnel support

Table 1. Basic Specifications of Mach-Three Intake Model

Item	Description
Format	Three-shock, mixed compression, rectangular crosssection, and attached air-drawing mechanism (open and close)
Ramp (First Wedge)	15°
Cowl (Second Wedge)	5° 9°
Throat Height	16.5 mm 15.4 mm
Opening Crosssectional Area	35 x 52.5 mm
Back Pressure Control	Movable flow plug method
Total Length	695 mm

On the side wall of the model, an optical glass is built in for Schlieren-observation of shocks. Pressure measurements were made at 84 points by a (Scanny) valve, variable dynamic pressure was measured at six points, and thermocouples at three points and a median layer behavior sensor (MP sensor) were used.

The examples shown in Figure 2 are the Schlieren photographs and their corresponding observation sketches for the model with the cowl angle of five degrees under the conditions of mach-three and open air-drawing valve. Shown in Figure 2 (1) is the state under the control of nearly proper back pressure. Two oblique shocks and a group of shocks, which have emerged in place of terminal shocks and which complicatedly intersect with each other in the vicinity of the throat, are visible in the photograph. A shear flow-like boundary can be seen in the region considered to be subsonic, causing a speculation for the presence of flow separation. The state depicted in Figure 2 (2) is of non-start by further tightening the flow plug and driving the shock group upstream from the throat. Several oblique shocks can be seen crossing each other in a complex fashion due to the flow separation in the crosssectional area near the cowl. These Schlieren pictures are suspected of being influenced by the flow's three-dimensionality, and further examination of the pictures in depth is necessary.

Our future objective is to establish the engine intake technology for SST, HST and space planes by continuing research to improve the intake's performance (at Mach-three and a pressure recovery coefficient of greater than 0.85) and its speed, as well as to provide variable shapes for the intake, through model testing, numerical analyses and basic experiments. (The Intake Research Association)

Gust Tunnel Data Processor

Improvement of Data Collection Section

The gust tunnel had, since its completion in 1972, been used in many research tests by both NAL groups and outsiders. The gust tunnel test data have been collected (by OKITAC-4300) and processed (by OKITAC-4500) in an off-line fashion through measurement devices equipped with their exclusive computers. In 1984, however, because of the devices' small capacity and slow processing speed, a graphic input/output processing computer (ECLIPSE S/140) was moved from the Computation Center (then called) to be used for these devices until today.

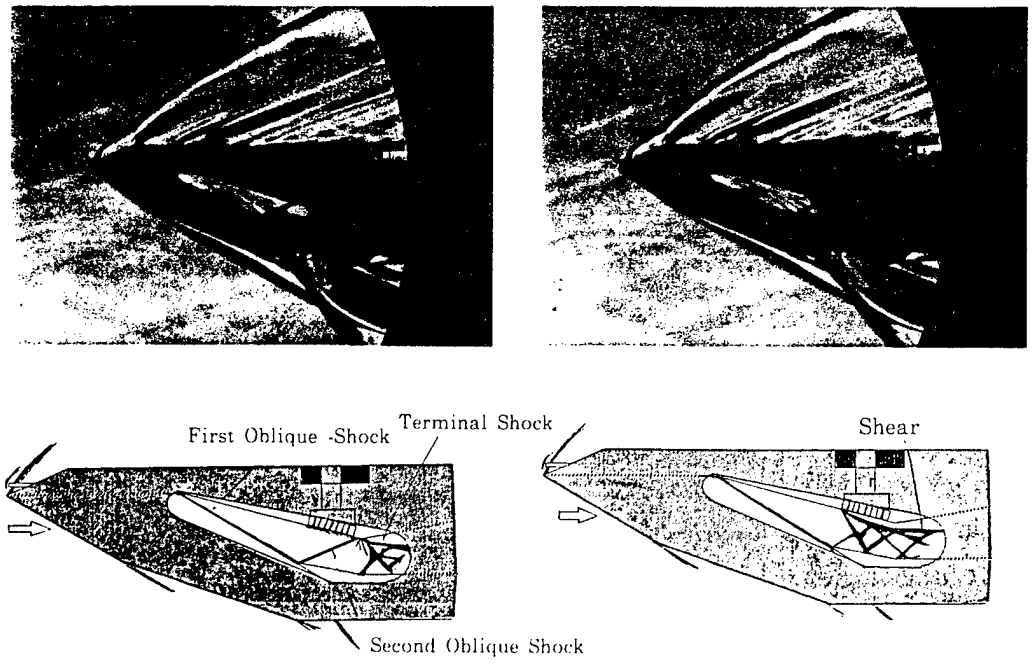


Figure 2. Shock Patterns at Mach 3

(1) State of nearly proper back-pressure
(2) State of high back-pressure and shocks driven upstream (non-start state)

It has been more than 15 years since the beginning of the operation of this device. As wind tunnel tests have become more diversified and more sophisticated, not only have the measurement devices become decrepit, but also the capability of processes, including the measurement data collection, has reached its limit with the format to record collected data directly on a magnetic tape and to calculate in an off-line fashion. Consequently, the tests ca no longer be executed smoothly. Recently, a new computer (ECLIPSE MV7800XP) has been installed through the FY87 special revised budget, and the data collection section has been improved. This report will discuss the summary of the attempt to improve the efficiencies in data collection and primary data processing for wind tunnel tests.

The following basic guidelines were used for the selection of a data collection computer in conjunction with this improvement program.

(1) The On-line format will be adopted to combine the collection and processing of data.

(2) The data collection and processing will be automated and real time CRT displays will be used for the results of primary processing in order to avoid retesting due to the occurrence of poor-quality data.

(3) Data can be transferred at a high speed (100 KB/SEC) to existing computers (ECLIPSE S/140) to cope with the secondary processing and output of massive data.

(4) The system must be able to accommodate the future expansion and reinforcement of sensors including the pressure measurement with ESP (electronically scanned pressure sensors) and the laser measurement of flows.

The outer appearance of this device is shown in Figure 1 and a diagramatic representation of its construction is given in Figure 2. This device uses an operating system (OS) called AOS/VS (advanced operating system/virtual storage). As many as 1,024 programs can be simultaneously run with this OS. Therefore, program development and debugging can be easily done parallel with a wind tunnel test. Furthermore, by elevating the measurement priority during a wind tunnel test, the test can proceed and data file can be protected without any influence from another user. Also in this device, a VME (Versa Module Europe) bus is used to form lines connecting various VME boards and the host CPU (Figure 3). The set-up and action directions for this VME bus can be done easily by using a VME handler under an AOS/VS FORTRAN77.

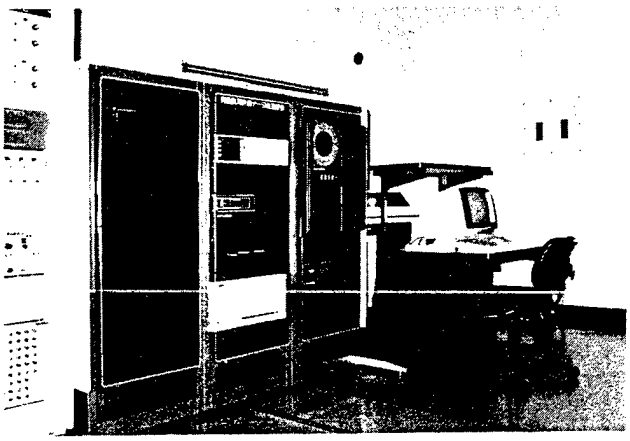


Figure 1. Gust Tunnel Data Processing Device

By this improvement, the measurement system has been completely renovated and the test efficiency has improved drastically through the improved productivity of wing tunnel test data due to the capabilities of on-line measurements and "quick-look" functions.

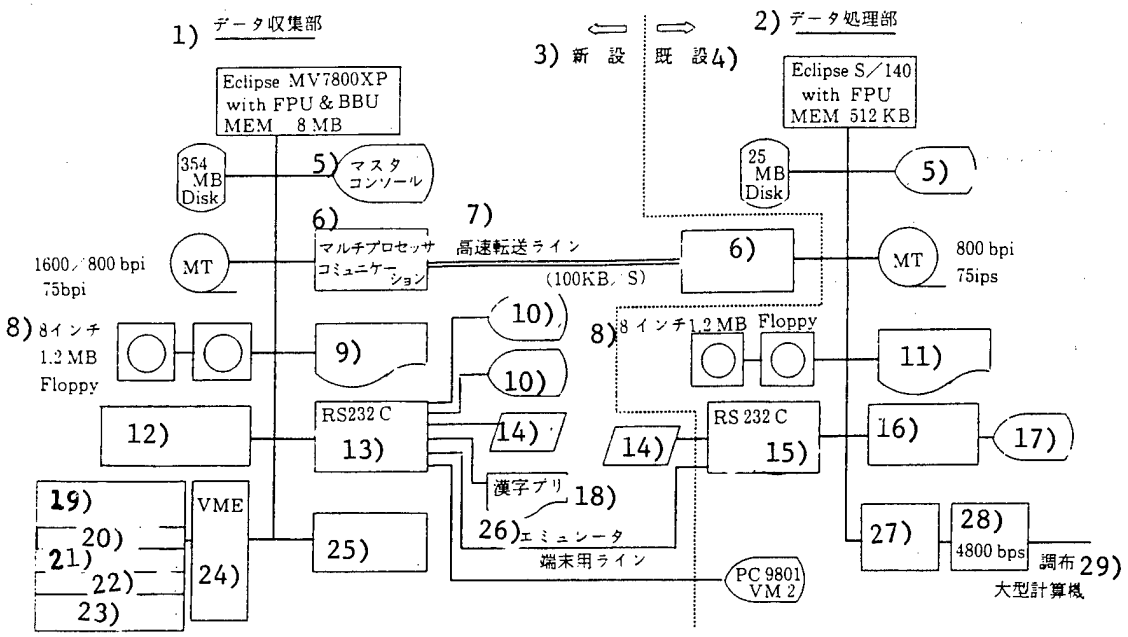


Figure 2. Schematic Diagram for Construction of Gust Tunnel Data Processing Device

(1) Data Collection Section
(2) Data Processing Section
(3) Newly installed part
(4) Existing part
(5) Master console
(6) Multiprocessor communication
(7) High-speed transfer line
(8) Eight-inch 1.2 MB Floppy
(9) Band printer 670 LMP
(10) Console
(11) Band printer 250 LPM
(12) High-speed A/D 3-ch, 14-bit, 100 KHz
(13) RS232C interface, 8-line
(14) Plotter
(15) RS232C interface, 4-line
(16) Console interface
(17) Second console
(18) Kanji printer
(19) Medium-speed A/D 32-ch, 14-bit, 50 KHz
(20) TTL input 160-point
(21) Contact point input 32-point
(22) TTL output 16-point
(23) OC output 64-point
(24) VME bus basic system
(25) High-speed GPIB interface
(26) Emulator terminal line
(27) Modem interface
(28) Modem 4,800 bps
(29) Large computer at Chofu

Today, progress is seen in the pressure measurement by ESP and the stream measurement by laser. We plan to update the measurement system by incorporating these technologies in the near future. (Group No 11, New Aircraft Research Group)

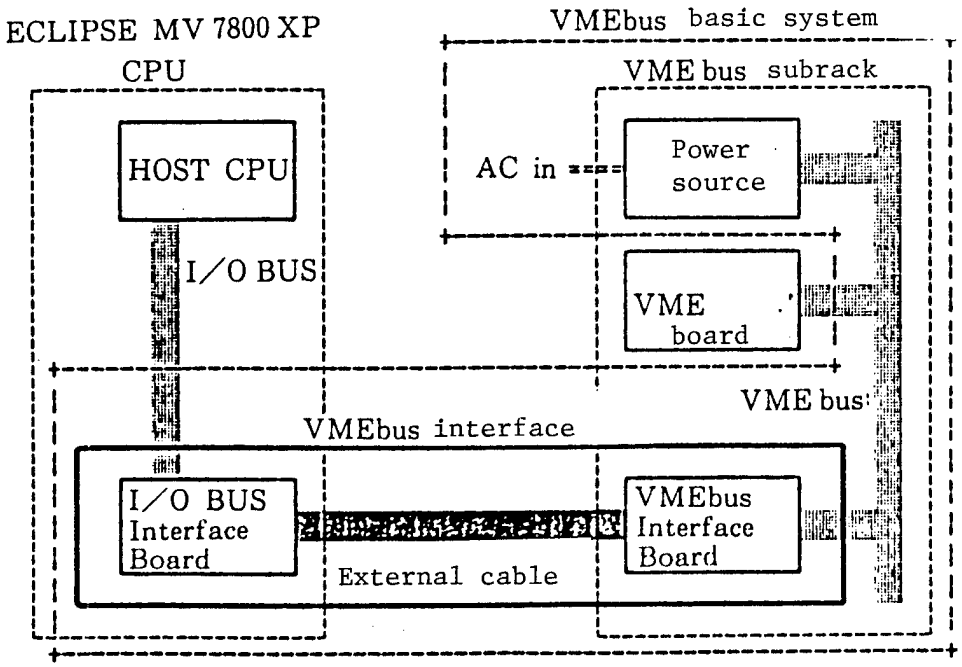


Figure 3. VME Lines

National Aerospace Lab News Reported

Space Plane's Aerodynamic Simulation

43062091 Tokyo KOGIKEN NYUSU in Japanese May 89 pp 2-4

[Article written by Yukimitsu Yamamoto, Aerodynamic Department]

[Text] A space plane assumes a wide range of angles of attitude from low to high elevations in superhigh speed regions of ascents and descents, and is subjected to severe aerodynamic heating during these times. Therefore, the clarification of the plane's aerodynamic characteristics is one of the most important projects for the airframe design. The Aerodynamic Department has done research on the ultrasupersonic flows around a space plane by means of numerical simulation using the (Nabie)-Stokes formula (see the Dec 87 issue of KOGIKEN NYUSU). In this article, several recent research accomplishments will be discussed. A surface pressure and isobar diagram at Mach 7.0 and an elevation of 50° is shown in Figure 1. By taking the wake region in the rear wing area with approximately 600,000 grid points, it was possible to calculate large angles of elevation. A comparison of a series of calculated values with test results at the National Aerospace Laboratory's (NAL) ultrasupersonic wind tunnel showed good agreements in aerodynamic constants and pressure distribution. Shown in Figure 2 is a cross-sectional isobar graph at Mach number 20.0 and zero degree of elevation; this is an example of an expanded Mach number region. Figure 3(a) illustrates a surface aerodynamic heat distribution for a space plane model with tip fins attached to it. High aerodynamic heating appears along the front edges of the tip fins under the conditions of Mach number 7.0 and zero angle of elevation. The graph in Figure 3(b) is an aerodynamic heat distribution at the fins' front edges and the top and bottom symmetrical surfaces from the nose to the rear end, corresponding to the situations depicted by Figure 3(a). Aerodynamic heat is expressed relative to the maximum value at the nose, the open circles in the graph indicate experimental values of aerodynamic heating as measured by the surface temperature determination method using infrared light. Parametric studies with angles of elevation up to 20° were carried out, using more than the above-mentioned model, for the numerical simulation of aerodynamic heating, in order to examine the effects of the swept-back angle of the fin's front edge and the effects of shock wave interferences. Two isobar graphs in Figure 4 are the results of simulation for a space plane equipped with an air intake

at Mach number 7.0 and zero angle of elevation. Inlet conditions were used as boundary conditions for the air intake. The future plan is to pursue the evaluation of aerodynamic performances of an engine-integrated space plane including (puruumu) calculation for an outlet nozzle.

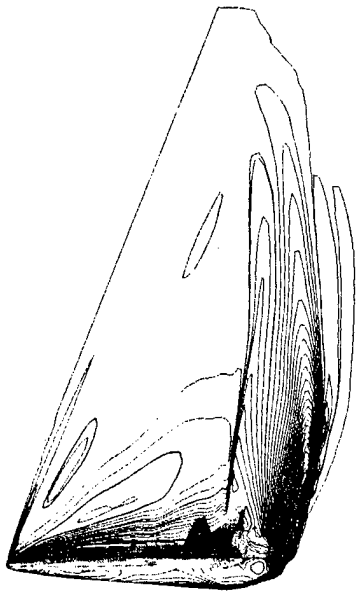


Figure 1. Isobar Graph Around Space Plane
($M\infty = 7.0$, $\alpha = 50°$, $Re\infty = 4.4 \times 10^6$)

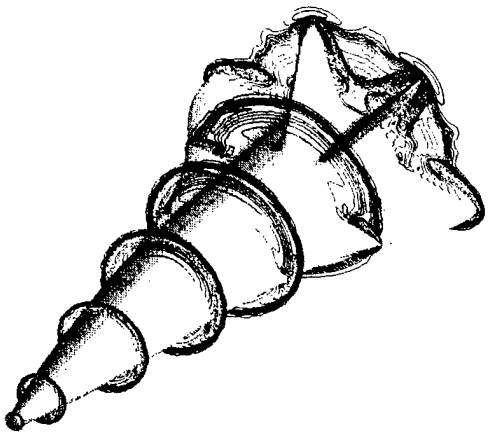


Figure 2. Cross-sectional Isobar Graph Around Space Plane
($M\infty = 20.0$, $\alpha = 0°$, $Re\infty = 1.3 \times 10^7$)

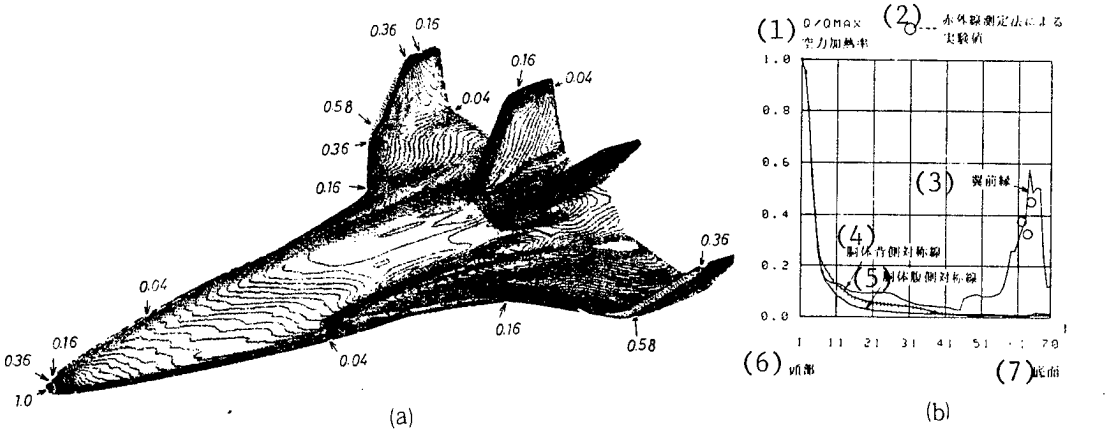


Figure 3. Surface Aerodynamic Heat Distribution on Tip-Finned Surface Plane
(M_∞ = 7.0, α = 0°, Re_∞ = 4.4 x 10^6)

Key:
(1) Q/Q_{MAX}, Relative Aerodynamic Heat
(2) Experimental Values per Infrared Method
(3) Fin's Front Edge
(4) Symmetric Lines at the Body's Top Side
(5) Symmetric Lines at the Body's Bottom Side
(6) Nose
(7) Bottom Surface

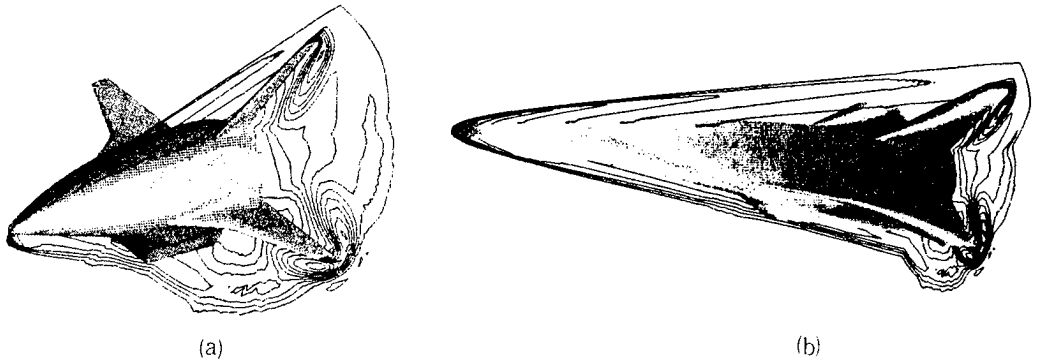


Figure 4. Isobar Graph Around Space Plane With Air Intake
(M_∞ = 7.0, α = 0°, Re_∞ = 4.4 x 10^6)

Prototype Stirling Engine for Space

43062091 Tokyo KOGIKEN NYUSU in Japanese May 89 pp 5-7

[Article written by Kunihisa Eguchi and Sachio Ogihara, Space Research Group]

[Text] The output of large electric power through a thermal generation system of more than 10 kW which uses space energy, such as sun light, is increasingly in demand as future space activities are trending toward expansion. Although thermal engines, thermal electrons or thermocouples can be used for this energy conversion, thermal engines are the choice as the promising thermal method that can hopefully effect weight reduction and efficiency improvement of an entire system compared with the previous solar ray generation. In fact, U.S. NASA's Lewis Research Center is carrying out a thermal generation technology program (SP-100) in an attempt to generate more than several hundred kW of power in the early part of the 21st century. Similarly, power conversion techniques using a thermal engine have been proposed and examined for future thermal generation systems at the European Space Agency (ESA) and in West Germany. The National Aerospace Laboratory has pursued basic studies concerning the thermal engine and the solar ray gathering-heat conveyance as a part ofthe research project on solar ray-gathering-type heat generation technology. In these studies, the Stirling engine has been chosen as a heat cycle engine that is expected to demonstrate high energy conversion efficiency and weight reduction. A small prototype Stirling generator model (NALSEM-125) was made and subjected to evaluation tests for the purpose of obtaining basic design data necessary for conforming the operation conditions in a space environment of microgravity and super vacuum. Shown in Figure 1 is the structure of the 125-W output engine generator (the first prototype) which was produced in FY88. The outside view of the entire engine is shown in Figure 2. This engine, unlike previous kinematic type engines which operate with mechanical link mechanisms, is a gamma, free piston type engine that generates output by the forced vibration mode of a spring-mass point system consisting of a gas spring space and a power piston and powered by pressure. The engine's cycle output is taken out as an electric power of a linear generator working as a load damper. An electric heater is used to heat the working gas, a water-cooled cooler is used for cooling, and a multi-layer mesh regenerator is used for heat regeneration in the cycle. The displacer piston, which moves the working gas between the expansion chamber and the compression chamber, is driven by a DC motor; the piston's frequency (i.e., the engine speed) and stroke can be changed. The average cycle pressure, the heating pipe temperature and the cooling water's inlet temperature have been chosen as input parameters during the engine operation. As indicated by the data processing flow shown in Figure 3, in order to acquire the graphic display capability on a P-V graph, pressure's cyclic changes and an average temperature ofthe working space were obtained, and electric inputs to the heater, heat required for cooling and the generator's outputs were simultaneously determined. These data were fed to a computer through a data logger and an FFT spectrum analyzer and displayed on a CRT. All performance data were saved on a hard disk. Shown in Figure 4 is an example of performance measurements in the forms of pressure variations

and P-V curves under input conditions of an average pressure at 2.0 MPa and a temperature ratio of 3.15. The phase angles ofthe displacer and the power piston were obtained from these pressure variation data and the display output was calculated by P-V integration for one cycle of expansion and compression of the space. The graph in Figure 5 shows examples of the internal power conversion efficiency (display work divided by expansion work) in the working space as obtained from a P-V diagram and the measured electric power generated by the linear generator. The two curves exhibit the dependency on the engine speed. Thus, the performance characteristics of the engine generator's output and efficiency were better understood, and ideas to improve display performances and to stabilize the vibration mode were acquired. The development of a performance computation program was started by combining a thermodynamic model and a vibrational model based on the analysis of experimental data.

The first prototype model, which was used in this study, was designed and produced with the cooperation of the Second Technical Development Research Institute of Aisini Seiki Co., Ltd.

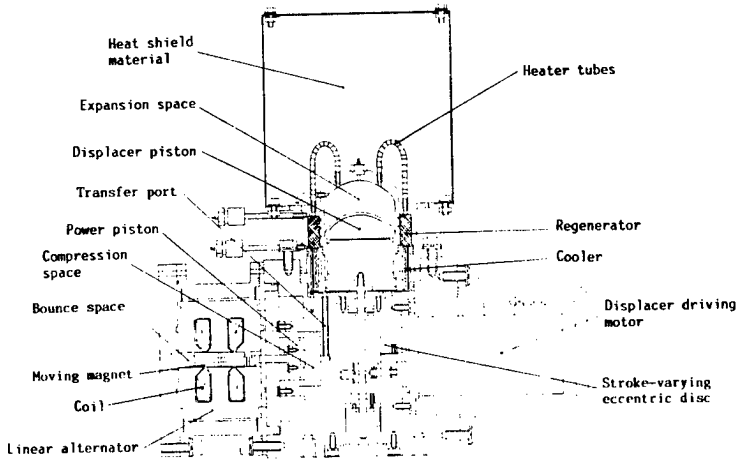


Figure 1. Structure of Stirling Engine Generator (NALSEM-125)

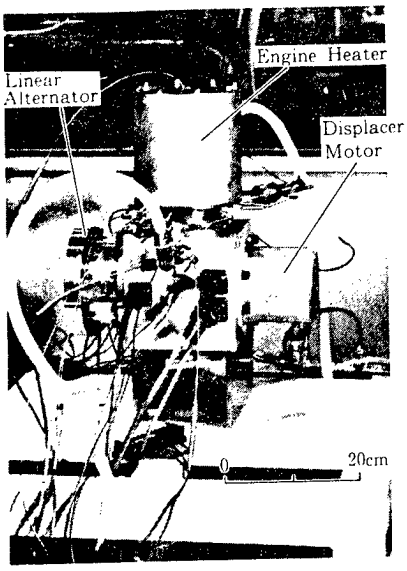


Figure 2. Outside View of Engine Generator

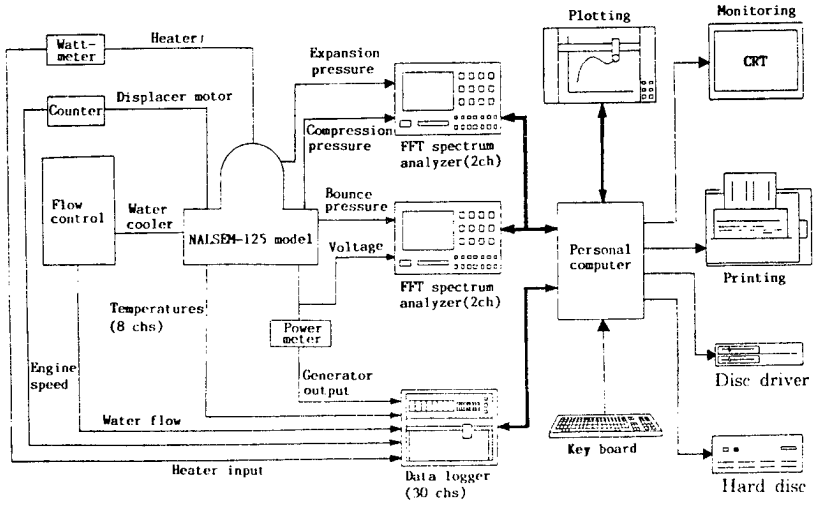


Figure 3. Data Processing System for Engine Performance

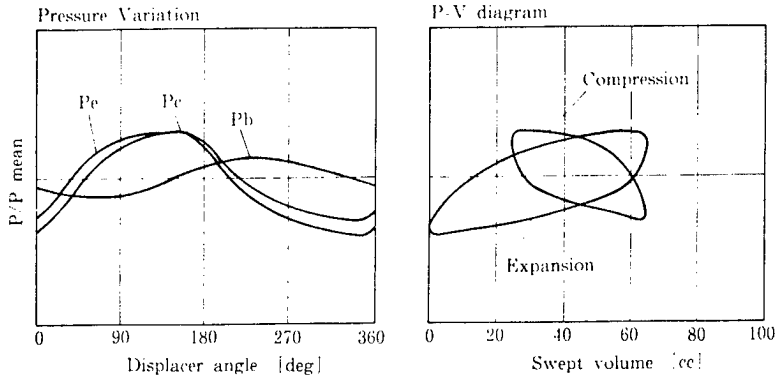


Figure 4. Pressure Variation and P-V Diagram for Working Space

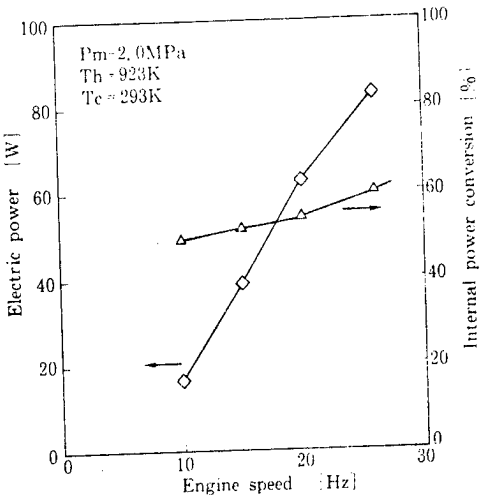


Figure 5. Internal Power Conversion Efficiency and Electric Power

FADEC Prototype for Ground Tests

43062091 Tokyo KOGIKEN NYUSU in Japanese May 89 pp 8-10

[Article written by the Motor Performance Research Laboratory, Motor Department]

[Text] FADEC, the acronym for Full Authority Digital Electronic Control, is a digital control for engine control variables including fuel feed and VSV angle. Today, this technique is becoming the mainstream for engine control. In particular, variable cycle engines and engines for SSTs and space planes contain many variable parts from the mechanistic standpoint. Therefore, the aid of computers is inevitably introduced for controlling these engines.

This article discusses a multi-CPU FADEC that we have test-produced to use in research work on the control software and signal processing and to use in ground tests of FJR engines.

The hardware system for this FADEC is shown in Figure 1. The sytem consists of the sensor section to sense engine information; the signal conditioner section to conversion-process the engine information to electric signals (analog quantity) and transmit them; the computation-control section to control the engine by computing electric signals after A/D conversion; and the FBU (flow body unit) to receive control signals and properly establish a fuel feed and a VSV angle.

The signal conditioner section converts engine information, including engine speed, temperature and pressure, to voltage, standardizes voltage readings, converts them to current for transmission, andagain converts current back to voltage for transmission to the computation-control section.

The computation-control section, one of the unique features of this FADEC, adapts a multi-CPU system by assigning tasks to three CPUs. In other words, the first CPU does the A/D conversion at a rate of 0.3125 ms/10 ch., removes noise by a filter through moving average of arbitrary lengths, and sends data through the digital I/O port.

The second CPU, receiving data from the first CPU, computes a fuel feed and a VSV angle which have been scheduled in response to the engine's working conditions and simultaneously sends target values every 20 ms while displaying the control quantities on the CRT. The third CPU, which receives these target values, in turn sends instructions every five ms to a torque motor (MV.S.V, VSV.S.V) of the FBU, as shown in Figure 2, and devotes itself in controlling the fuel metering valve and the VSV angle.

For the selection of CPU, the PC-9801VX was chosen because of the easy availability of peripheral devices, the organized environment for software development, and the best understood internal structure.

The FBU was manufactured by Ishikawajima-Harima Heavy Industries Co., Ltd. to be equipped with functions equal to or better than the FCU (fuel control unit) of an FJR engine.

NAL handled the design through production for the development of the signal conditioner and the software.

Having completed tests concerning the characteristics of the FBU, we are now testing with an FJR engine. As an example of test results, a photograph of CRT screen at the engine start is shown in Figure 3. The target values for the metering valve (the white line) are shown almost on the schedule (the blue line), and the target values for the fuel feed (the red line) also show good agreement.

In the future, we plan to use this FADEC to clarify various phenomena occurring at the start of an FJR engine.

FADEC BLOCK DISGRAM

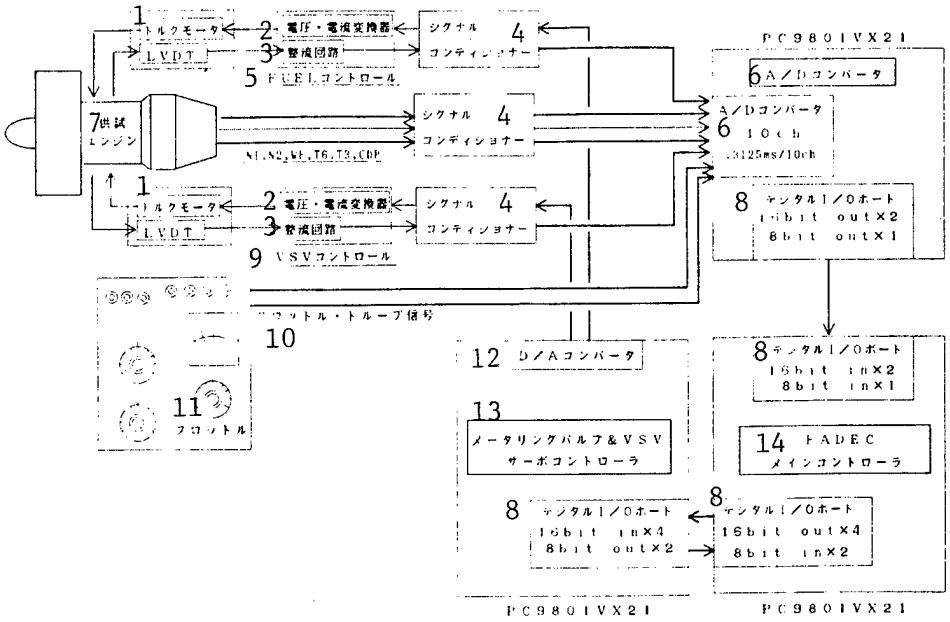
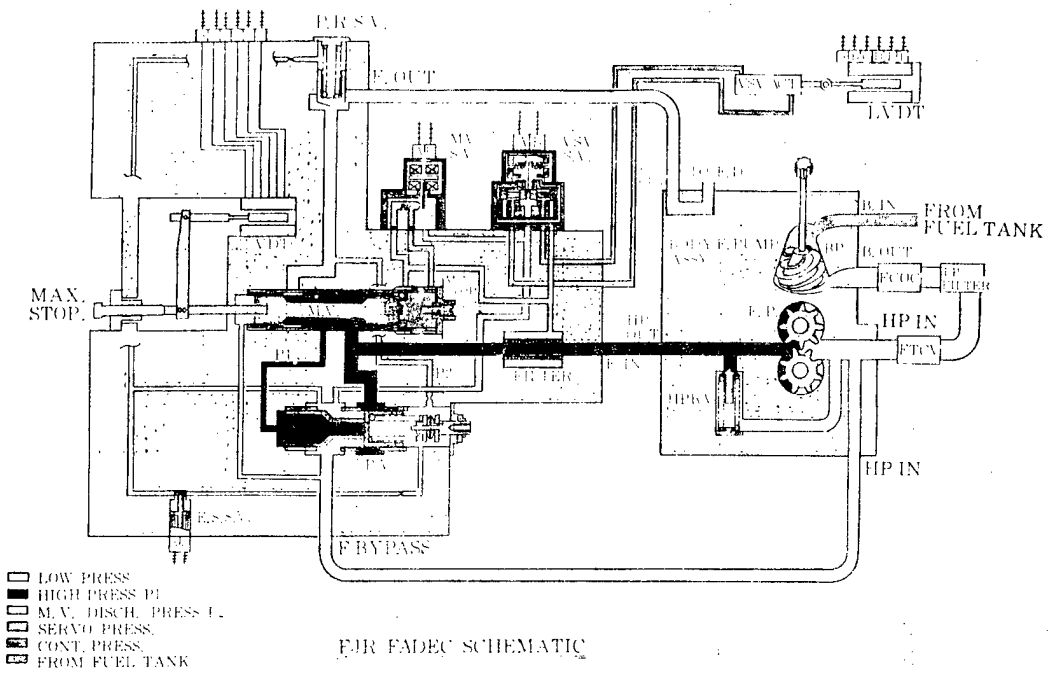


Figure 1. FADEC System Diagram

Key:

1. Torque Motor
2. Voltage-Current Converter
3. Rectifying Circuit
4. Signal Conditioner
5. FUEL Control
6. A/D Converter
7. Engine under Test
8. Digital I/O Port
9. VSV Control
10. Throttle Droop Signals
11. Throttle
12. D/A Converter
13. Metering Valve & VSV Servo Controller
14. FADEC Main Controller



FJR FADEC SCHEMATIC

Figure 2. FBU Conceptual Diagram

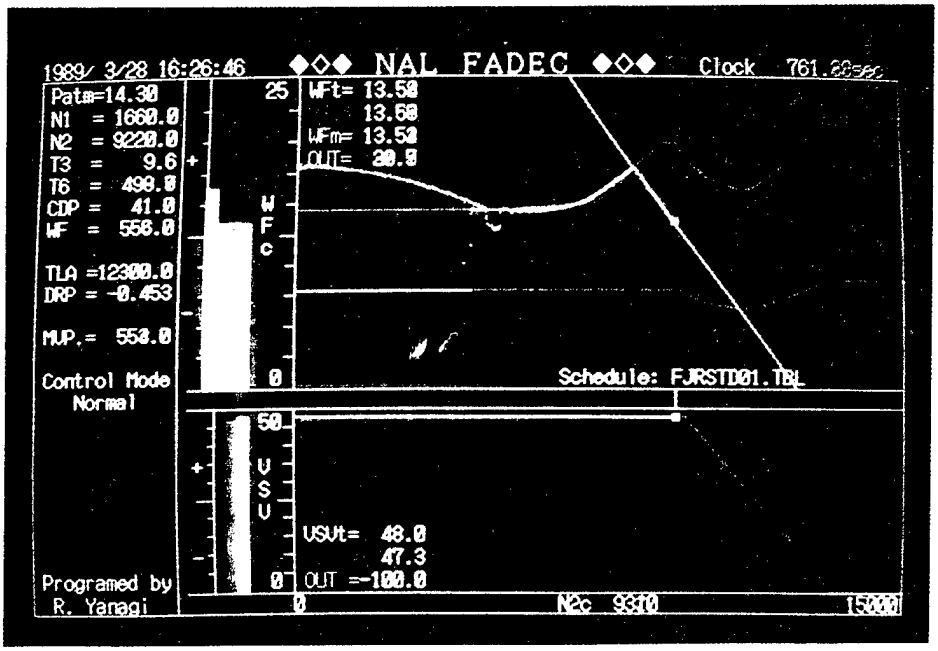


Figure 3. CRT Screen

Japan to Develop Flight-Control Software for FSX

43065216 Beijing JISUANJI SHIJIE [CHINA COMPUTERWORLD] in Chinese No 30, 2 Aug 89 p 10

[Unattributed article: "Japan to Independently Develop FSX Flight-Control Software"]

[Summary] Japan wants to independently develop the flight-control software for the disputed FSX fighter plane, even if this might cause the earliest active service date of the fighter to be delayed two years or more. The source code for the fighter's digital flight-control software is a critical item denied to Japan during the Bush government's early-1989 discussions on amending the co-production agreement. Recently, the Japan Air Self-Defense Forces (JASDF) and the Japan Defense Agency decided that Japan would independently develop this software, although the entire system could be purchased in "black-box" [i.e., sealed] form from the U.S. It is still not clear who will undertake the software research on this project, but JASDF has decided on this course of action since, if Japan does not develop this software, it can lose a critical part of its technological development work. Initial estimates are that this developmental project will require over two years of effort; this would postpone the earliest in-service date from the original target of 1994 to 1996 or later.

Recent Developments in VLSI Etching Technology

Low-Temperature Ion Etching

43064069 Tokyo SEMICON NEWS in Japanese Oct 88 pp 22-25

[Report by Keiji Horioka, Tsunetoshi Arikado, Makoto Sekine, and Haruo Okano, ULSI Laboratory, Toshiba Corp.: "Low-Temperature Reactive Ion Etching--High Selective Ratio Etching of n+poly-Si"]

[Text] 1. Introduction

The integration of LSI devices is making further progress with the support of developments in fine patterning technology, and competition in the development of a 16M DRAM has already started. With the reduction in design rule, in particular, requirements for etching techniques focusing on the following five points--processing forms, selectivity, speed, uniformity, and low damage--are becoming increasingly severe.

Especially in the processing of n+poly-Si, a gate electrode material that is most important in the MOS transistor manufacturing process, even a slight change in gate length leads to a fluctuation in threshold voltage and, moreover, causes the thickness of the gate oxide film to fall below 100Å. Therefore, higher processing accuracy and selectivity than hitherto are required. For this reason, we explored the use of low-temperature RIE for cooling a substrate to less than 0°C in order to make such processing forms compatible with selectivity.

2. Low-Temperature, High-Selective Ratio Etching of n+poly-Si

2.1. Etching Equipment and Test Samples

Figure 1 shows the structure of the magnetron RIE equipment used for our research.

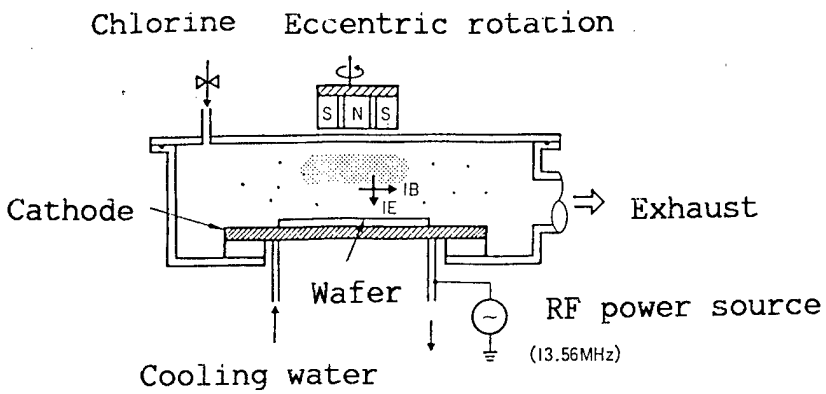


Figure 1. Magnetron RIE equipment.

A wafer is put on a cathode to which RF power is to be applied, and a permanent magnet in the form of a concentric circle is placed on the reverse side of an anode. The parallel components of the magnetic field arising from this magnet between the cathode and the anode, plus the effect of an electric field orthogonal to these components, cause electrons to start a cycloidal motion, and thus a high-density magnetron plasma is formed. The ions in the high-density plasma are extracted by the electric field in the sheath and collide with the wafer, making it possible to effect very rapid, highly directional etching. The self-bias voltage arising in the cathode stands at about 100V, lower than in the case of ordinary RIE of the cathode coupling type, and makes low-damage etching possible.

A flow path for cooling purposes is provided in the cathode, and a cooled fluorine gas or a nitrogen gas is allowed to flow and cooled below the freezing point. The wafer is fixed with an electrostatic chuck, and heat transfer between it and the cathode is ensured by He gas.

As etching samples we used phosphorus-added n+poly-Si, formed by the CVD method, and thermally oxidized film.

2.2. High Selective Ratio Etching and Its Mechanism

Figure 2 shows the dependence of etching speed upon temperature in the form of an Arrhenius plot.

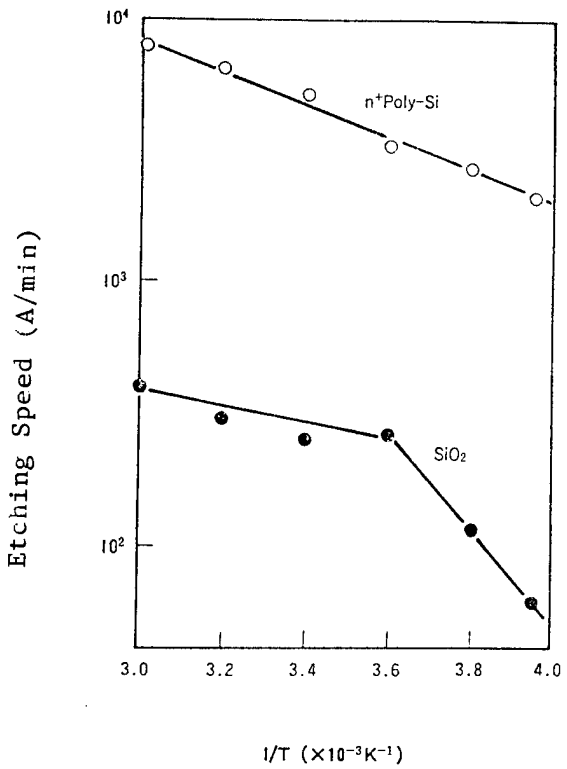


Figure 2. Dependence of etching speed upon temperature.

The etching gas is chlorine, and the pressure is 0.01Torr. As is clear from the illustration, the speed of n+poly-Si etching drops linearly with a fall in temperature, whereas the speed of SiO_2 etching turns downward at 0 °C and drops rapidly therefrom. As a result, the selective ratio of n+poly-Si to SiO_2 increases markedly and reaches more than 100 at -40 °C.

We measured the XPS on the SiO_2 surface to ascertain the cause of the fall in SiO_2 etching speed. Figure 3 shows a comparison of the Si2p peaks on the SiO_2 surface etched at room temperature and at -20°C.

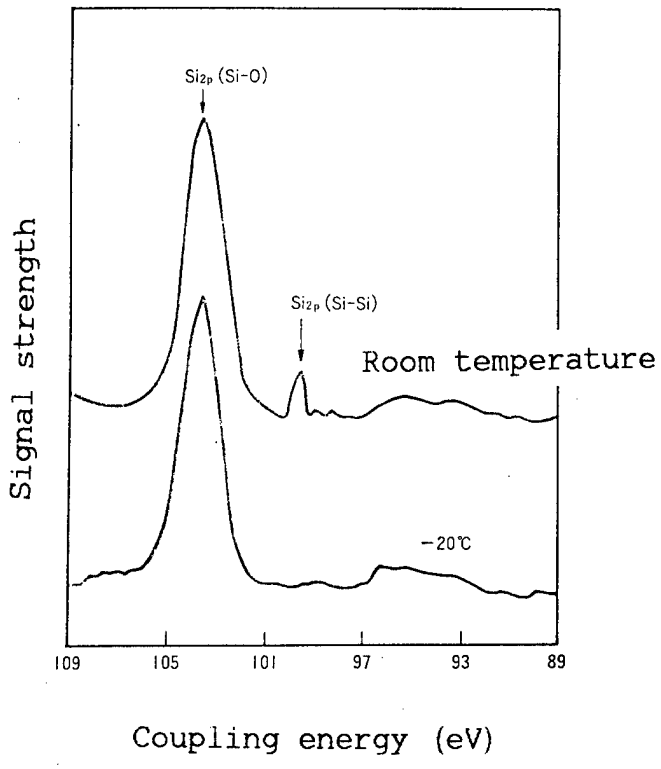


Figure 3. XPS spectrums on SiO_2 surface after RIE.

From the SiO_2 surface etched at room temperature, a small signal caused by an elemental Si is recognized at 98eV, in addition to an Si2p peak (102eV) in an oxidized state. This result indicates that the Si on the SiO_2 surface is partially resolved--a common phenomenon in the case of a surface shocked by charged particles such as ions and electrons. From the surface etched at -20°C, however, no peak of any elemental Si is detected. This suggests that there is a protective layer on the SiO_2 film at -20°C, preventing the surface from being directly exposed to ion shock.

We thought that such a surface protective layer might be produced as a result of condensation of SiClx or SiClxOy, a product of Si or SiO_2 etching, formed on the cooled SiO_2 surface. Both the Si-O and Si-Cl combinations exhibit a comparatively strong ionic nature. Therefore, it is conceivable that an etching product containing such a combination would be preferentially condensed on an SiO_2 surface having a higher degree of ionic bond that a covalent n+poly-Si surface.

To confirm such selectivity, therefore, we carried out an experiment by discharging and $SiCl_4$ gas and oxygen at 0.05Torr. We found that both n+poly-Si and SiO_2 were etched at room temperature. At -20°C, on the other hand, only n+poly-Si was etched; chlorine-containing films in the state of an oxidized film were selectively accumulated on the SiO_2,

preventing the progress of etching. This result supports the above-mentioned model.

The condensation of a protective layer on the SiO_2 surface takes place through its equilibrium with the etching product in a gaseous phase. Therefore, the effect of protecting SiO_2 cannot be expected even at low temperature unless it is under more than a given pressure (10^{-2}Torr level). Figure 4 shows the dependence of etching speed on substrate temperature under 10^{-3}Torr. Under such a low pressure, the speed of SiO_2 etching does not fall even at low temperature. It is generally constant in a range between -40°C and 60°C, and the selective ratio is only about 5.

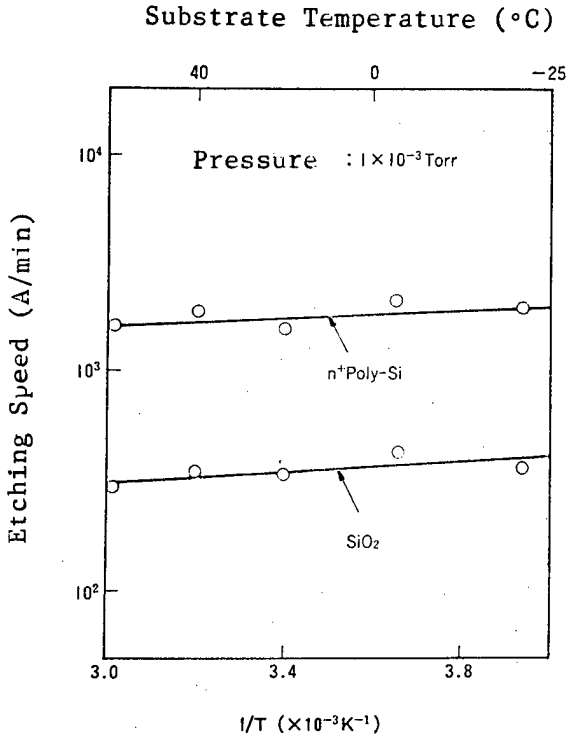


Figure 4. Dependence on temperature under 10^{-3}Torr.

2.3. n+poly-Si Etching by Three-Layer Resist Mask

In the case of lithography below the level of 0.5μm, excimer laser and electron beams are thought to be effective means of exposure. Since the resist exposed to them is not very tolerant to plasma, use of multilayer resist technology is unavoidable.

When n+poly-Si is isotropically etched through its reaction to the chloric atoms in plasma, a substance arising from the resist resolution due to ion shock sticks to the resist side-wall and acts to prevent an

undercut. A plane on which ions are slantwise incident has a higher physical sputtering effect than that on which ions are vertically incident. Therefore, a slightly tapering resist side-wall is the best source of films that protect the side-wall. However, as the side-wall of a multilayer resist is vertical, the amount of resist resolution is small, and this tends to bring about an undercut.

One effective way to inhibit this undercut is to lower the etching pressure and reduce the partial pressure of chloric atoms. Under low pressure, however, no condensed layer appears on the SiO_2 surface, as previously stated, and this makes it impossible to obtain a high selective ratio.

Therefore, we added $SiCl_4$ and O_2 gas to raise the partial pressure of SiClx and SiClxOy in a gaseous phase for the purpose of securing a high selective ratio even at low pressure. Figure 5 shows a comparison of etching speed between Cl_2 gas (100%) and Cl_2+$SiCl_4$(15%)O_2(1%) mixed gas.

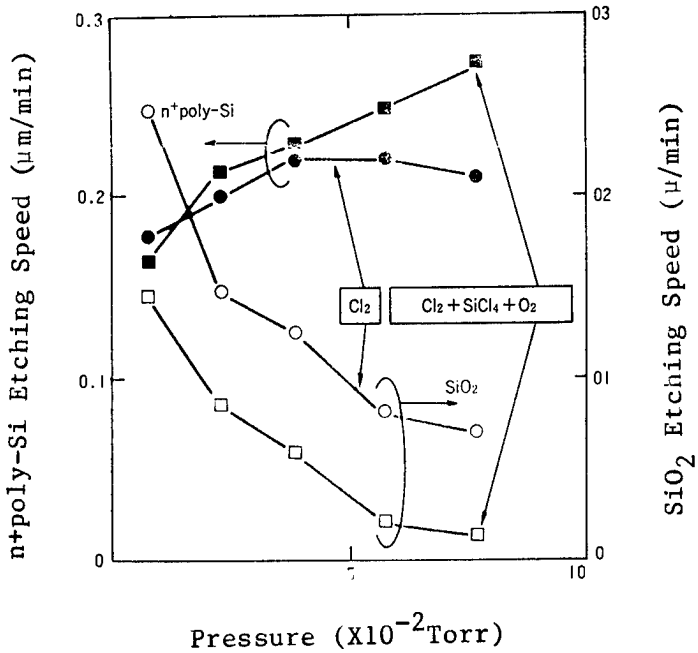


Figure 5. Etching speed and pressure using Cl_2 gas and Cl_2 + $SiCl_4$ + O_2 gas.

The n+poly-Si etching speed made no great difference no matter which gas was used, while the SiO_2 etching speed dropped under all pressure, as expected, with the addition of $SiCl_4$ and O_2 gas. As a result, we obtained a higher selective ratio even under low pressure that brings about no undercut.

Photo 1 [not reproduced] shows a processed form of n+poly-Si etched at -15°C using this gas. An anisotropic form of processing and a high selective ratio of 40 compared with SiO_2 were achieved even when a three-layer resist was used.

For the purpose of confirming the superiority of etching showing such a high selective ratio, we trial-manufactured an MOS transistor, with an n+poly-Si electrode and gate oxide film measuring 3,500A and 100A in thickness, respectively, and the gate measuring 1μm in length. In terms of room temperature (selective ratio: 10) and -20°C (selective ratio: 40), we carried out 100 percent overetching, respectively. Figure 6 shows the I-V characteristics of the transistor.

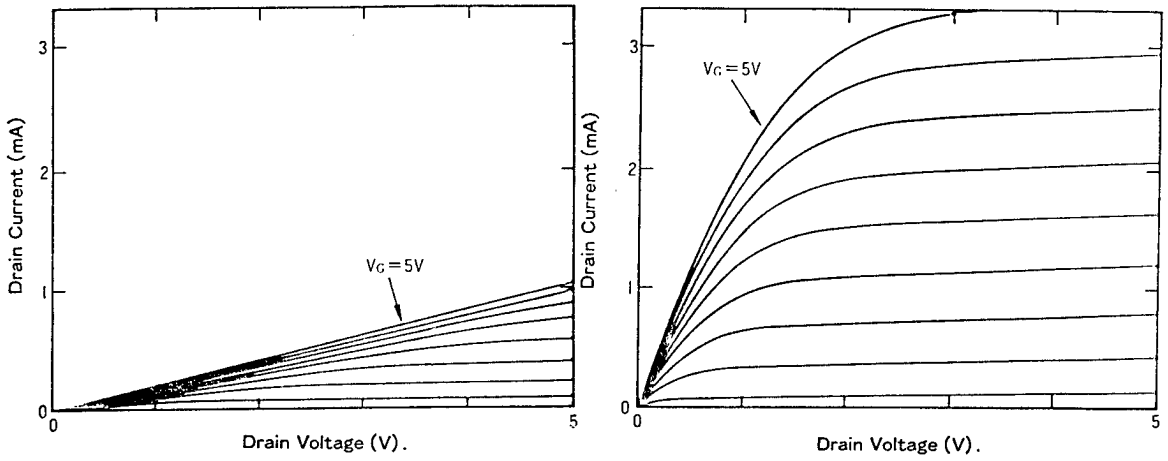


Figure 6. I-V characteristics of trial-manufactured MOSFET.

When the selective ratio is low, the gate oxide film is etched completely, with the etching extending even down to the Si substrate. As a result, a vertical step is produced between the source-drain area formed by ion injection and the channel area. This causes a strong parasitic resistance because the amount of ion injection is small on the side-wall of the step, and also because the inversion layer due to the gate electric field does not reach the side-wall. Therefore, only a slight channel current is obtained, as shown in Figure 6 (a), making the thinning of the gate oxide film unimportant. On the other hand, etching at a high selective ratio makes it possible to obtain normal I-V characteristics, as shown in Figure 6 (b).

3. Conclusion

We have devised an n+poly-Si etching technology requiring the cooling of a silicon wafer below 0°C and use of anisotropic and highly selective plasma, applicable even to a process using a multilayer resist as a mask. We also trial-manufactured an MOS transistor and confirmed the

effectiveness of this technology for the manufacture of submicron devices for the near future.

Etching Technology, Equipment Trends

43064069 Tokyo SEMICON NEWS in Japanese Oct 88 pp 31-37

[Report by Hiroyuki Okada, Kyoto Laboratory, Matsushita Electronics Corporation: "Latest Trends in Etching Technology, Equipment"]

[Text] 1. Introduction

The integration of semiconductor devices is advancing at an increasingly rapid pace, and various companies, after offering 4M DRAM samples, have entered the submicron age on the mass-production level.

To date, the accuracy of fine patterning has been determined by the limit of stepper resolution, but due to the improvement of steppers and resist processes, dry etching and CVD methods have become key technologies in determining whether devices for the future are appropriate on an 0.8-micron mass-production level. The physical analysis technology for the in-line evaluation of processed devices has also become an important factor not only as a peripheral technology but also as a manufacturing technology.

The important tasks for etching technology include improvement of reproducibility of silicon etching, which is necessary for trench separation and for the formation of trench capacitors; reduction of contamination and damage; aluminum etching with high-density Cu added to prevent migration; measures to prevent corrosion; and adoption of an etching method involving little plasma damage, which has become a problem with the thinning of device films.

As means of accomplishing these tasks, remarkable progress has been made in ECR etching for which microwaves are used, magnetron etching (MRIE) by use of a magnetic field, low-temperature etching for the cooling of wafers, etc.

Here I will describe the current status and trends in the dry etching technology used for the processing of silicon semiconductors.

2. Trends in Etching Technology

The technological tasks in carrying out fine patterning are summed up in Table 1. In the case of chargeup during an etching process, which brings about dielectric breakdown in gate oxide film, in protective film and in interlayer film, it is necessary to lower the density of electric power and isolate the wafer from the cathode.

Table 1. Problems Involved in Etching, Countermeasures

Item	Effects on Devices	Countermeasures
Chargeup	Unsatisfactory withstand voltage for gate oxide film. Short circuit between aluminum and substrate. Unsatisfactory open circuit.	Lowering the density of power. Insulating the RF electrode.
Contamination	Shift of Vth. Deterioration of hFE and gm. Leakage. Increase in contact resistance. Deterioration of capacitors.	High-purity insulation coating of electrode and reaction chamber. Applying low ion energy. Cleaning the surface after etching. Providing etching conditions using accumulated film that is easy to remove.
Damage	Shift of Vth. Deterioration of hFE and gm. Leakage. Increase in contact resistance. Deterioration of breakdown voltage. Deterioration of capacitors.	Annealing at high temperature and for a long time. Applying low-ion energy. Removing the surface after etching.
Particles	Fall in yield.	Improving the cleaning method and frequency. Adopting etching conditions involving little accumulation. Using gas, piping, materials for a reaction chamber and a processing method, all involving little dust.

To cope with contamination that degrades device properties, it is necessary to take such steps as increasing the purity of the electrode materials and providing etching conditions involving a small amount of accumulated film.

In the case of sputtering damage that causes crystal defects, it is necessary to remove the damaged layer by means of etching or to anneal it at high temperature for a long time. When this is difficult from the viewpoint of a process, the ion energy for etching must be lowered.

With regard to particles, which are the biggest cause of a drop in yield, it is necessary to improve the method and frequency of cleaning, as well as to improve the structure of equipment and provide conditions inhibiting the generation of dust.

Next I will describe the current status of some dry etching technologies, including aluminum etching and trench etching, and I will discuss general problems involved in the manufacture of devices.

2-1. Aluminum Etching

For the past several years, there have been many announcements concerning aluminum etching, because aluminum wiring with high-density Cu added is essential to obtain high reliability in regard to migration. There are broadly two problems involved in the addition of Cu to aluminum. One is that this tends to give rise to etching residua because of the low vapor pressure of Cu chloride, and the other is that the residual chlorine tends to bring about corrosion. In regard to removing the residua, it is possible to raise the water temperature during the etching process and to increase the sputtering energy, if the selective ratio to resist is sacrificed to some extent. As for corrosion, however, checking into the method of aftertreatment is an important task. With regard to the occurrence of erosion, two types--(a) globular corrosion and (b) aluminum deficiency--are known. Globular corrosion is caused by moisture in the air, as shown in Figure 1 (a), and therefore a method often used to prevent this is to form a strong, fluoride passivation film on the side-wall after aluminum etching by using the gas plasma of phlorocarbon, in order to prevent the aluminum surface from direct contact with the outside air. The aluminum deficiency takes place when the resist is removed. As shown in Figure 1 (b), it is caused by the action of the residual chlorine on the wafer and a large amount of water, and therefore it is necessary to reduce the amount of residual chlorine as much as possible and also to inactivate the aluminum surface by fluorinating or oxidizing it. As to the problem of corrosion, it is difficult to evaluate on a quantitative basis because of poor reproducibility. There are many tasks to be tackled in this connection, such as checking into etching conditions with little residual chlorine and improving the method of aftertreatment.

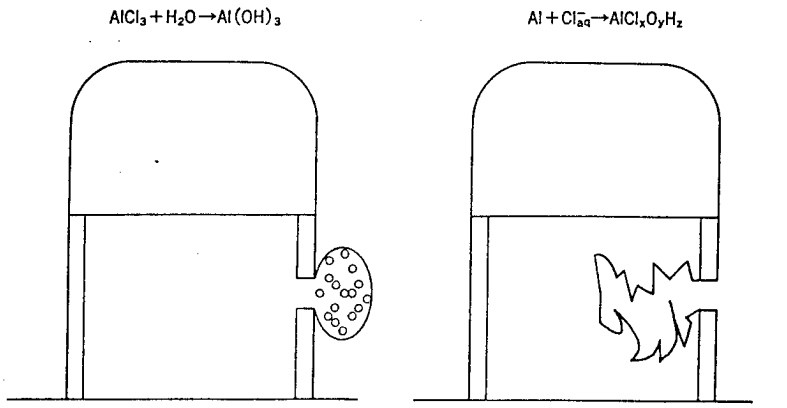


Figure 1. Types of aluminum corrosion.

As for aluminum wiring, barrier metals are indispensable with the diminishing of contact holes and the thinning of impurity diffusion layers. As barrier metal materials, Ti, TiW, TiN, W, silicide, etc., are used, but the conditions for using them are complex because the films to be etched are multilayered. Also, since different kinds of metals contact each other, they readily bring about corrosion due to battery effects.

In any case, in the case of submicron rule wiring etching, the films to be etched are different from the conventional ones. Therefore, it is necessary to review the current technology bearing in mind the basis of plasma reaction, and as to equipment, to create a unit etching system of a multichamber type covering a wide range of applications, including multilayered film etching, passivation, and resist removal.

2-2. Gate Etching

In the etching of submicron gates, the size shift must be held at zero, and as to the substrate oxide film, a high selective ratio is necessary because the film becomes as thin as less than 10nm. Also, as the aspect ratio becomes higher, the dependence of the etching depth and form upon the pattern width, which is well known in trench etching with a high aspect ratio, comes to be observed in gate etching, too, depending upon the nature of the mask pattern. It is therefore necessary to effect etching with the condition of strong anisotropy. However, it is difficult to achieve simultaneously a high selective ratio to the substrate. As a measure to cope with this, studies are being conducted to obtain a higher selective ratio by cooling the wafer to less than 0°C and utilizing the adsorption of gas to the substrate, or to effect anisotropic, high-selectivity etching by using high-temperature chloric gas beams instead of plasma.

In conventional RIE at normal temperature, it is difficult to obtain the necessary selective ratio to the substrate--20 or more--under the etching condition of holding the size shift at zero. However, the selective ratio can be raised to 30 or more by cooling the wafer to -20°C. Putting this to practical use involves many tasks, such as the handling of a piping system designed to cool the equipment and resolving the problem of water adsorption after the removal of the wafer. However, the use of this method is advantageous in that it can be investigated from the scope of conventional technology. As a gate electrode material for the future, high-melting-point metallic polyside is widely used because of the demand for a lower resistance ratio. However, it is difficult to etch silicide-polysilicon two-layer film, and no satisfactory result has yet been obtained. In this regard, a low-temperature etching technology is thought to be useful, and it can be expected that the application of the conventional RIE method will become widespread.

In gate etching by means of ECR, a low ion energy is used in a high vacuum, making it easy to obtain anisotropy. Use of this process also enables independent control of the microwave power that controls the density of etchant, as well as the bias RF power that largely influences the selective ratio. This makes it easy to achieve a higher selective ratio. However, because of the high ion density that is an advantage of ECR, there is also the problem of the gate electrode charging up during the etching process and making the gate insulation film liable to break. It is necessary to study conditions for reducing the chargeup by combining this formula with low-temperature etching.

2-3. Trench Etching

For the 4M DRAM, of which samples have begun to be shipped, many manufacturers use trench capacitors. In the case of etching silicon trenches, unlike the etching of thin film, the terminuses cannot be detected during the etching process, and the trenches and holes to be formed have 5-10 aspect ratios and 3-5 micron depths, respectively. Therefore, it is very difficult to conduct examinations. Equipment for conducting nondestructive examination of trench forms with SEM is being developed by means of image processing, but there are many problems in introducing it to a manufacturing line. Therefore, a great deal of effort has been made to achieve the stability and mass-productivity of silicon etching. When the conventional RIE method is used, it is difficult to form a silicon trench with a high aspect ratio and good reproducibility. Figure 2 shows problems often encountered in trench etching. Defects due to unstable etching conditions, such as microtrenches and bowing, and also due to deviation in a preceding process, such as silicon blacks and surface defects, must also be covered by etching. Bowing and microtrenches, caused by excess radicals or a reactive gas absorbed on an etching surface, can be eliminated by cooling the wafer. Silicon blacks and surface defects are caused by the laminate film or spontaneously oxidized film at the time of oxide film

etching, which is the preceding process. Therefore, it is necessary to work out a way of treatment to be carried out before silicon etching.

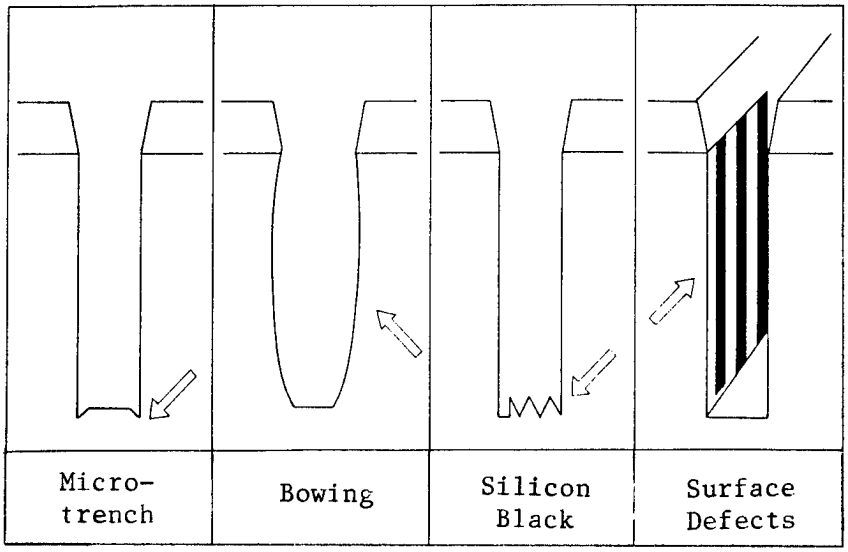


Figure 2. Poor modes of trench etching.

Also, since an active device is created by forming a thin insulation film on the etching plane, it is necessary to take sufficient measures against etching damage and contamination, too. To reduce etching damage, it is necessary to weaken the energy of ions. RIE, however, is not practical because it causes the speed of etching to drop when the ion energy is lowered. This can be covered by RIE (MRIE: magnetron enhanced RIE) using a magnetic field and ECR (electron cyclotron resonance) using microwaves.

MRIE and ECR, which make it possible to obtain high-density ions in a high vacuum, facilitate the achievement of anisotropy. However, as it is difficult to completely restrain anisotropic components with these methods, it is necessary to study them in combination with low-temperature etching.

2-4. Oxide Film Etching

When a steep side-wall is formed in creating submicron contact holes, a hollow and wire disconnection arise, as shown in Figure 3 (a), because of the poor coverage of aluminum deposition. This results in a marked decline in device reliability, such as is seen in electromigration.

The selective growth of selective epitaxial growth of W has been under study for some time, but it will still be a while before such growth is put to practical use. Also, to improve the coverage, many efforts are being made for tapering or rounding during the etching process, as shown

in Figure 3 (b). However, the method of using resist recession involves difficulty in attaining reproducibility, and it is not suitable for mass production. There is also the method of tapering through the use of accumulated gas or lowering the apparent aspect ratio in combination with isotropic etching.

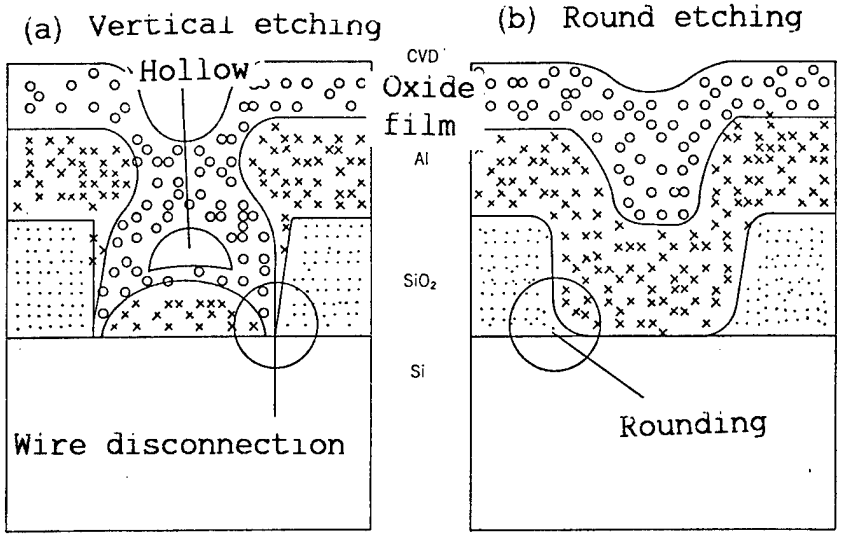


Figure 3. Relationship between contact etching and aluminum CVD coverage.

In the formation of a contact, the impurity junction becomes less deep, and therefore it is necessary to raise the selective ratio to silicon in the case of etching. A selective ratio of 10~20 is necessary, as against the current ratio of 5~10. If the selective ratio is raised by increasing the amount of accumulated gas, laminate film will remain in a contact hole or an accumulated substance will be pushed into a silicon substrate, causing the contact to become defective. One method of removing the surface layer by means of etching before aluminum evaporation is the use of a fluorine radical. However, as the impurity diffusion layer is as shallow as about 0.2micron, it will become impossible to adopt this method in the future. Therefore, it is necessary to establish an etching condition to reduce the sputtering energy and the extent of cumulative film formation. The controllability of equipment for cathode fall voltage, etc., must also be improved.

2-5. Ashing

There are many processes for resist ashing, and the processing conditions are simple, so batch processing has been adopted. Figure 4 (a) shows a typical specimen of the standard asher of a barrel type. However, the problem has arisen that with the thinning of gate oxide film, insulation film is destroyed by static electricity because of chargeup during the ashing process. There is also the problem of ion

implantation causing a silicon substrate to be contaminated by heavy metal from the resist material or the like. Therefore, a number of damage-free ashers involving little chargeup have appeared recently. They can be roughly grouped as (1) a downflow asher using microwaves (Figure 4 (b)), (2) an induction-type asher with a separate plasma generating chamber (Figure 4 (c)), (3) an ozone asher, and (4) a UV ozone asher with far ultraviolet rays added to ozone for the purpose of enhancing reactivity (Figure 4 (b)).

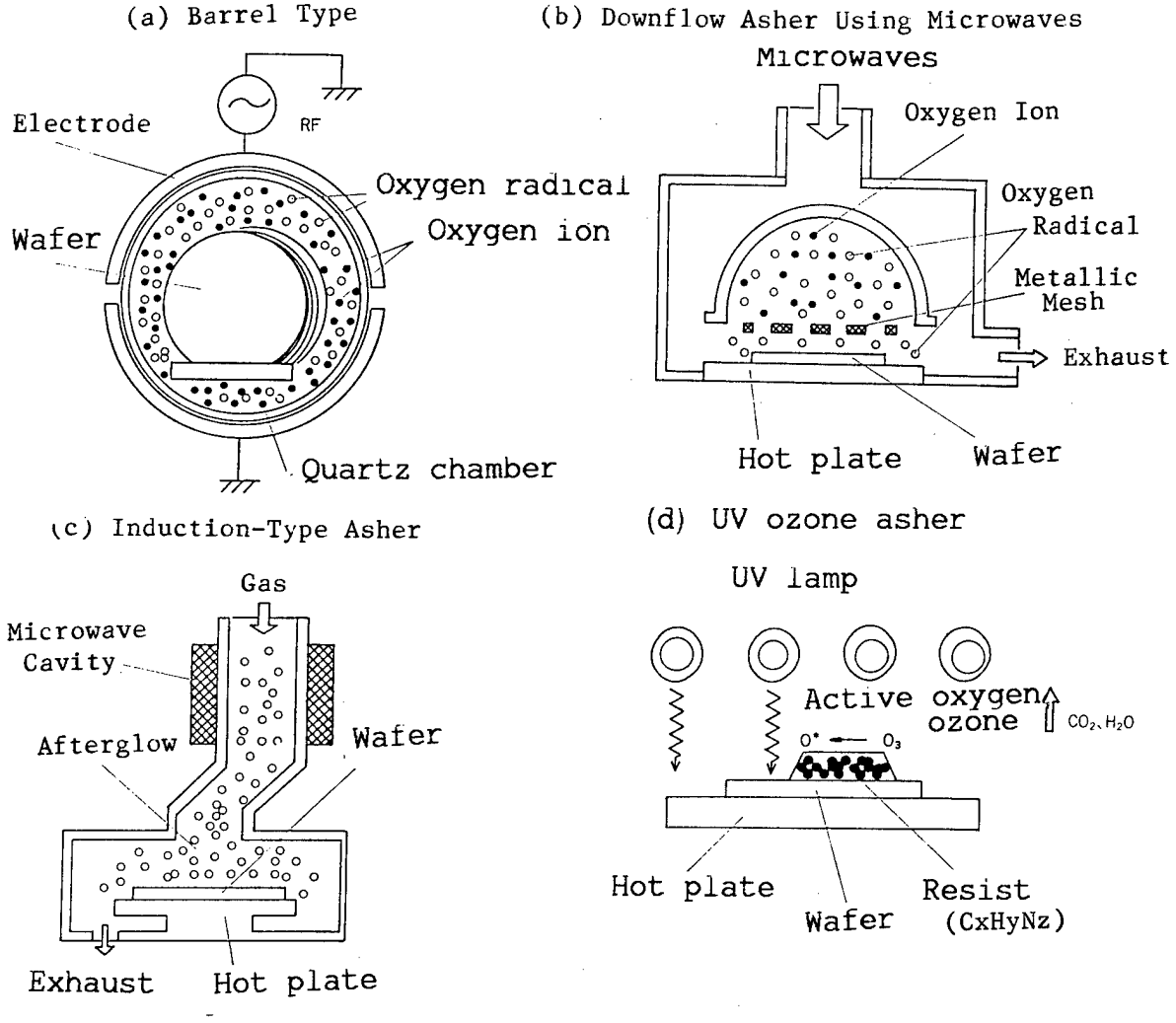


Figure 4. Typical specimens of various ashers.

All these have a structure whereby the ion is not allowed to come into direct contact with the wafer so as to avoid chargeup. These damage-free ashers are designed mainly for a radical reaction of oxygen, and therefore the wafer must be heated to 200°C～300°C during the ashing

process. An effort has also been made to effect ashing at low temperature by adding a gas, but this is not suitable for mass-production because the ashing speed is low.

3. Etching Equipment

Table 2 [on following page] shows a comparison of various kinds of etching equipment. PPE (parallel-plate-type plasma etching equipment) and RIE are currently used in most etching processes because they are easy to handle and knowhow has been accumulated. On the submicron level, however, damage and contamination, which were not a very serious problem previously, have become an issue, as mentioned earlier in connection with trench and gate etching. Thus, MRIE and ECR, which can be expected to help improve the basic properties of etching directionality and selectivity, are about to replace PPE and RIE. In this chapter I will report on these new kinds of etching equipment that will become increasingly important.

MRIE was initially put to practical use as a high-speed etcher of oxide film and silicon. Figure 5 shows a typical MRIE specimen. As this formula causes plasma to be closed up by a magnetic field, it is possible to obtain high-density ions with low power, and through this closure to avoid contact between the plasma and the outer wall of the reaction chamber.

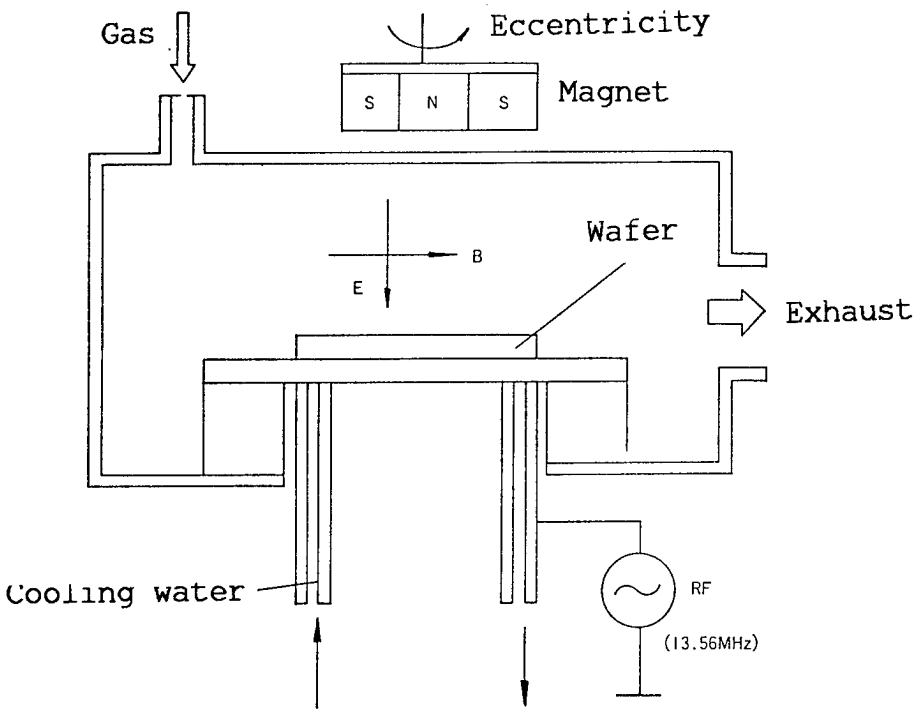


Figure 5. Typical example of magnetron etcher (MRIE).

Table 2. Comparison of Various Dry Etching Methods as to Performance

Item	Optical Etching	PPE	RIE	TRIODE	MRIE	ECR
Method of impression	Light	RF	RF	RF + RF	RF + magnetic field	ECR + RF
Pressure (Torr)	1～10	0.1～10	0.05～1	0.01～1	0.001 + 0.05	0.001～0.05
Directionality	Anisotropic	Quasi-anisotropic; isotropic	Anisotropic; quasi-anisotropic	Anisotropic; quasi-anisotropic	Anisotropic; quasi-anisotropic	Anisotropic; quasi-anisotropic
Selectivity	High	Medium	Medium	Medium	High～medium	High～medium
Etching speed	Low	Medium	Medium～low	Medium～low	High	Medium～low
Damage	None	Existent	Existent	Big	Existent	Existent
Contamination	Slight	Existent	Existent	Large	Small	Small
Extent of use	x	◎	◎	x	x	△
Future importance	x	△	○	△	◎	◎

This makes it possible to reduce the contamination of heavy metals. With the RIE method, a stable plasma arises even under low pressure--several mTorr--and this inhibits electric discharge. Therefore, it is easy to obtain anisotropy and, moreover, the high ion density brings about an increase in etching speed, an advantage for mass production.

As the wafer temperature rises because the plasma is closed up near the wafer by the magnetic field, it is cooled by means of an electrostatic chuck or a clamp. The use of the electrostatic chuck is a disadvantage from the viewpoint of reliability, and the use of the clamp makes the wafer carrying system complex. In the case of using an accumulated gas, the generation of dust (particles) becomes a problem. As mentioned earlier concerning gate and trench etching, lowering the temperature of the etching equipment is the trend of the future, and therefore, improving the cooling system is an important task in further promoting the practical use of MRIE.

Figure 6 shows a typical specimen of ECR etching equipment.

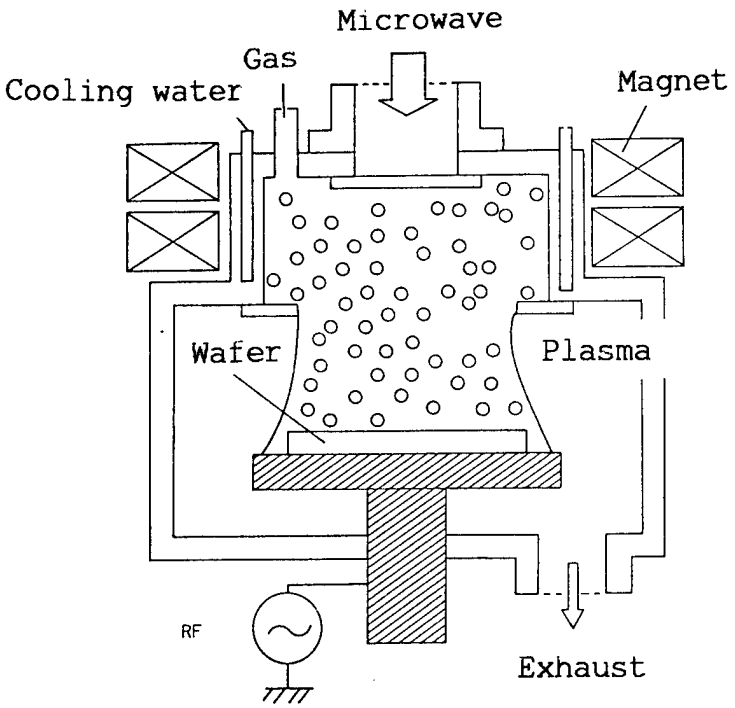


Figure 6. Typical example of ECR etcher.

The ECR etcher is designed to generate plasma by resonating 2.45GHz microwaves in a 875gauss field. As electricity is discharged without any electrode, it is possible to cut off the supply of any contaminated

substance arising from other than a reactive gas. The RIBE (reactive ion beam etching) system closely resembles the ECR etcher. This formula, however, needs a pull-out electrode, and is therefore disadvantageous for preventing contamination. There is also a limit to the density of ions that can be pulled out. ECR etching accelerates ions with the auto-potential formed by a divergent magnetic field, and therefore it can resolve the problem encountered in RIBE.

As the ECR etching equipment can also use a corrosive gas such as chlorine, it covers a wide range of applications. However, the auto-potential formed by ECR is as low as 10-20eV, causing the anisotropy to decline at normal temperature because of radical components. The anisotropy is improved by the strong impression of an RF bias, but the selective ratio falls because of the increase in sputtering energy. However, complete anisotropy can be achieved without using an accumulated gas by restraining the radical reaction almost completely through cooling the wafer temperature to -130°C, as in the case of MRIE. In this case, too, the formula for raising the wafer cooling efficiency remains a difficult issue, but ECR, like MRIE, is superior to RIE in reducing contamination. Therefore, the development of equipment to be mass-produced with an eye to lower temperature is earnestly desired.

In the case of ECR, practice has so far preceded theory, but analyses separated from parameters have achieved gradual progress. It can therefore be expected that ECR equipment will be developed wherein theory is reconciled with practice, so it can be applied to a mass-production line for the future.

4. Peripheral Technology

It is important to improve not only the etching properties but also the peripheral technology. With regard to dust control, which is the biggest factor in determining yield, there is as yet a lot of dust in the equipment, in spite of the fact that cleanrooms are about to attain a zero-dust level. It is therefore necessary to further improve piping and chamber materials as well as dust filters. It is also necessary to develop a construction technology to prevent the generation of dust or to make it easy to remove dust.

As for the vacuum pump that has been the biggest bottleneck in the preservation of equipment, the dry pump has generally reached the stage of practical use and is being freed from the problem of oil exchange. In regard to high vacuum exhaust, too, the turbomolecular pump has eliminated the fear of contamination due to oil mist or the like.

As for evaluation technology, various measuring apparatuses superior in accuracy and throughput are on the market for size measurements, which are an important item for the management of etching properties, and they are operating on the mass-production line. As mentioned in regard to

trench etching, however, observing the form of a device is an important item of management when it is three-dimensional.

There is currently no way but to observe a section of a wafer by cutting it, and this is a bottleneck in carrying out mass production. Eliminating this bottleneck is an important task for the future.

5. Summary

Greeting the age of submicron-level mass production, I have thus far dwelt upon the current status of etching technology and tasks to be tackled in this connection. Figure 7 [on following page] shows ways of carrying out the development of equipment in the future to cope with the growing complexity of process and evaluation technologies.

The propriety of semiconductors is still determined only by whether or not the equipment to be used is appropriate, and development and improvement of the equipment occupy an important position. To date, the main task of process technicians has been to evaluate the equipment put on the market, but with the required processes becoming increasingly complex, it has become imperative to adapt the equipment to individual processes and devices. Since the evaluation technology has also become more complex than ever, with greater weight given to knowhow, it has become necessary to depart from a situation wherein equipment developed with ideas alone may be a success or a failure, and to establish a setup whereby makers of equipment as well as devices can undertake joint efforts for the creation of equipment.

6. Conclusion

In this report I have described the trends of etching technologies and equipment as I see them. I will be happy if this is of some help to you, readers.

Trench Etching Technology

43064069 Tokyo SEMICON NEWS in Japanese Oct 88 pp 39-43

[Report by Masahiro Yoneda and Kyusaku Nishioka, LSI Laboratory, Mitsubishi Electric Corp.]

[Text] 1. Introduction

Devices of three-dimensional structure are being developed with the fining of pattern size and the enhancement of integration. As part of this development, a trench capacitor structure to increase the capacitor area by forming fine trenches on a silicon substrate and using these trenches as part of the capacitor, and a trench separation formula replacing the conventional LOCOS separation process by the selective oxidation method, are being applied particularly to IC's using bipolar transistors. As these trenches have come to be made infinitesimal and

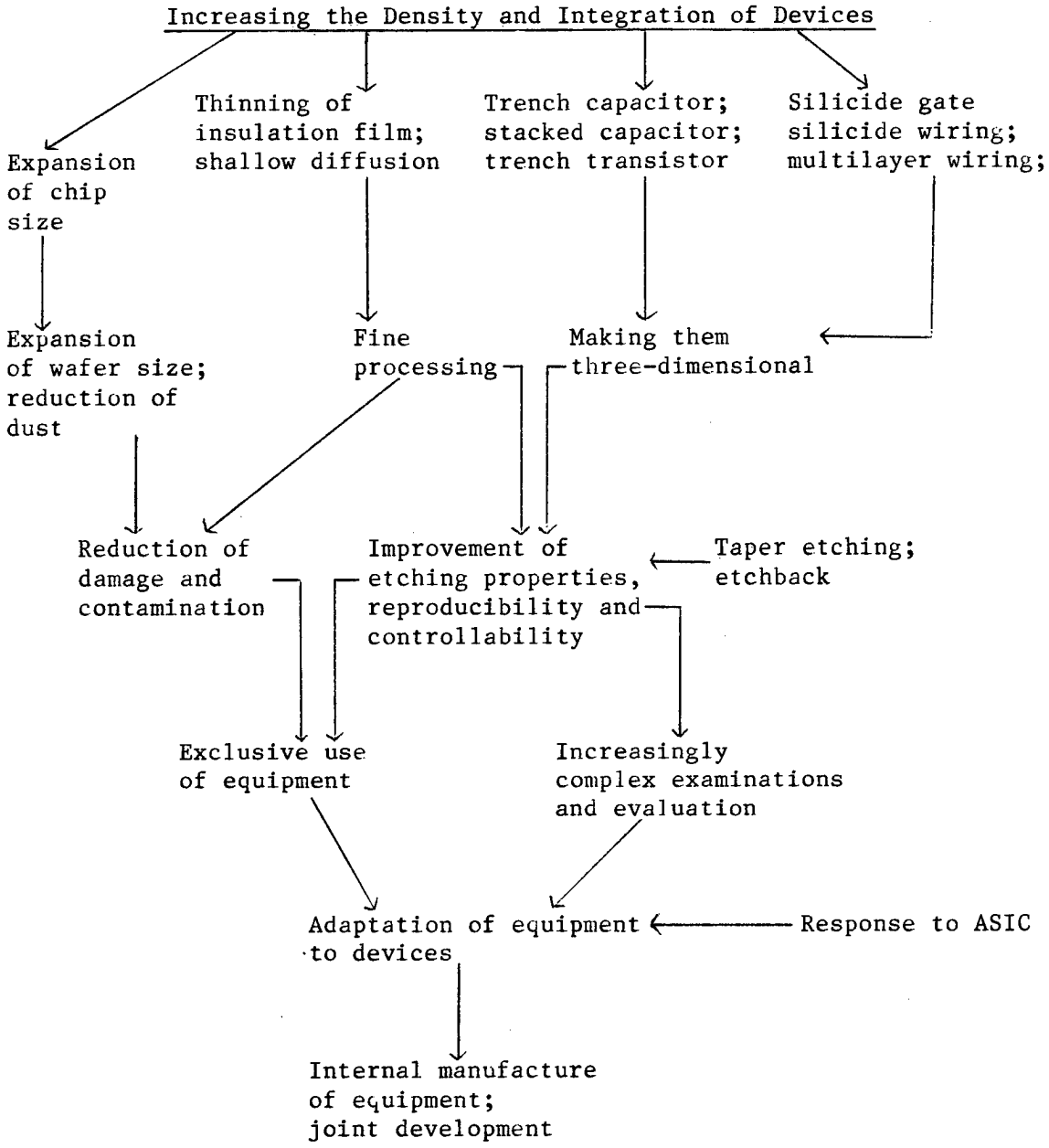


Figure 7. Trends of etching technology and equipment development.

given a high aspect ratio, they have to be processed very precisely with a silicon anisotropic etching technology (trench fabrication technology). Since a high aspect ratio is required in this technology, it is necessary for these trenches to have a generally vertical profile. It is also required that the etching plane be smooth, that the fluctuation in etching speed due to the difference in aperture size be held down to a low level, and that damage caused at the time of silicon etching can be removed easily.

Here we will introduce high-precision trench etching technologies that will meet ULSI requirements in the future.

2. Silicon Trench Fabrication Technologies

With regard to silicon trench etching, various etching methods are being explored at present. Various reports have been made on such methods as the conventional RIE formula, the double excitation RIE formula, the low-pressure RIE formula of the magnetic field impression type, and the ECR etching formula. Each formula has its advantages, but here we will focus on eliminating the defects of RIE, which is the most conventional etching formula, such as the low etching speed, the low selective ratio, and profile deterioration due to the trench having a high aspect ratio, by remodeling them so as to generate a high self-bias voltage in the cathode.

3. Etching With High-Bias Voltage Formula

In the case of RIE, DC negative voltage arises automatically on the cathode side on which high-frequency electric power is applied. The value of this voltage is determined by gas composition, pressure, impressed high-frequency electric power, etc. To give full play to this characteristic, the electrode and so forth are improved so as to bring about a state in which a stable glow discharge can be obtained even under low pressure. This state is used for trench etching.

Low pressure, high bias voltage, and a gas composition without Cl_2 gas provide etching conditions making it entirely possible to form a trench with a high aspect ratio. The basic gas composition consists of $SiCl_4 + N_2$, and this has so far been regarded as involving a problem in etching speed and selective ratio. The process of etching under low pressure and high bias voltage has the defect that a subtrench tends to be formed when Cl_2 is used as the main etching gas, and the addition of BCl_3 causes an increase in the speed of etching SiO_2 film that serves as an etching mask. That is why the above-mentioned gas composition has been adopted. This etching process makes it possible to form a satisfactory trench exhibiting a high aspect ratio without bringing about a defect on the surface of its side-walls or a subtrench.

However, when this is considered in connection with an actual device, the dependence of the etching area on the wafer surface presents a

problem. Figure 1 shows the dependence placed upon the etching area by etching speed, uniformity and selectivity.

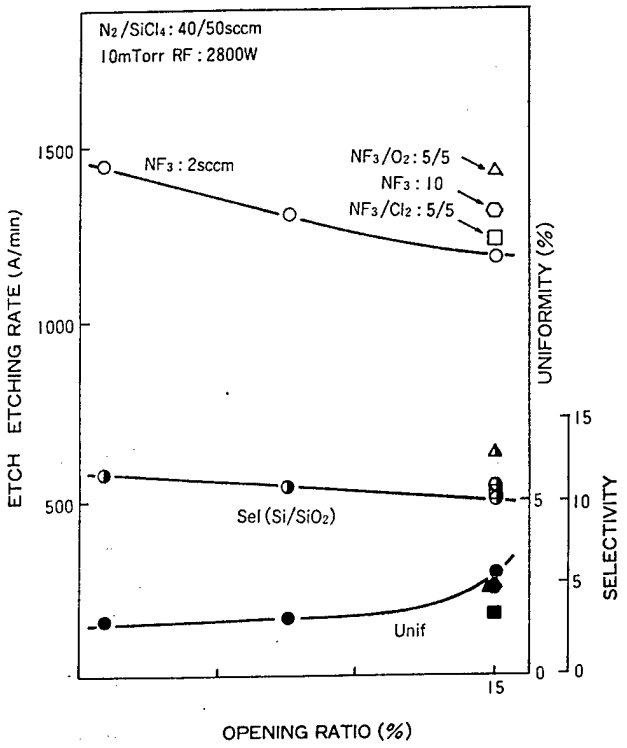


Figure 1. Dependence of etching speed upon opening ratio.

As etching is effected under low pressure, the etchant supply becomes insufficient when the etching area is increased, resulting in a fall in etching speed. This is accompanied by the tapering of the trench profile, probably due to an increase in the amount of reactive products. Figure 2 shows a SEM photo [not reproduced] of the trench profile observed when NF_3 is added to the basic gas composition. When the etching area accounts for 1 percent, the side-wall protecting film is evidently removed under the influence of F, and bowing appears. However, when the etching area constitutes 15 percent, an etching profile is formed with a taper angle of 87 degrees, conversely, because of a strong side-wall protecting effect. This means that when the etching area is wide, accounting for 15 percent or so, the profile can be controlled by adding a gas such as F or O which has the effect of removing the side-wall protecting film. This makes it possible to improve etching speed as well, as can be seen from Figure 1.

Figure 3 shows changes in the etching speed standardized by the etching speed exhibited when the trench size is 1μm, both in the case of etching under the conditions of high pressure and low bias voltage with BCl_3+Cl_2 used as an etching gas, and in the case of etching under the conditions

of low pressure and high bias voltage with N_2+$SiCl_4$ gas used as an etching gas.

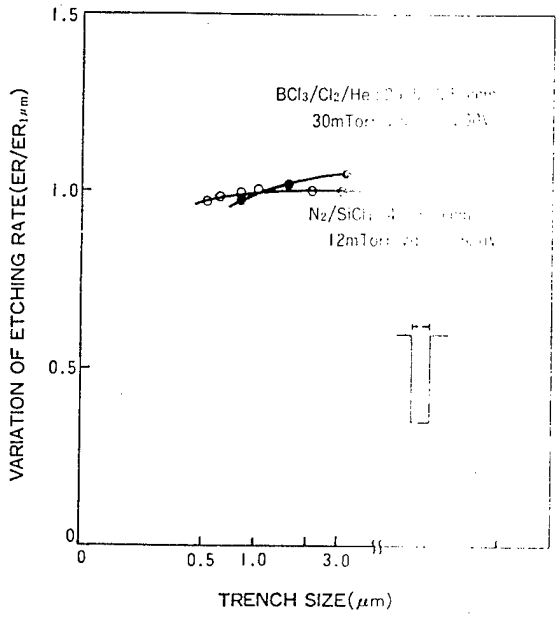


Figure 3. Microloading effects under various etching conditions.

Compared with a trench size of 1μm, under low bias voltage the etching speed undergoes a marked change with a different trench size: +15 percent in the case of 10μm in trench size and -2 percent in the case of 0.8μm. Under high bias voltage, on the other hand, the range of fluctuation is very small: +0.5 percent and -0.5 percent, respectively, indicating that the microloading effect is held down. This reveals that the etching in this case, achieved in terms of high bias voltage and low pressure, makes it possible to obtain an etchant involving a high degree of ion acceleration and satisfactory directionality. In light of this, the possibility is strong that adoption of a formula whereby a high etching speed under lower pressure is obtained will become the mainstream in trench etching in the future.

4. Damage Caused in Etching

With regard to trench etching, it has been found necessary to carry out etching under low pressure and high bias voltage in order to form a trench with a high aspect ratio. However, as the acceleration of ions, i.e., etchants, becomes strong in this case, there is fear of its causing serious damage to the silicon surface to be etched. Figure 4 shows the values of damage measurements using the thermal wave method when sacrifice oxidation was carried out under various conditions before and after etching, and after etching alone.

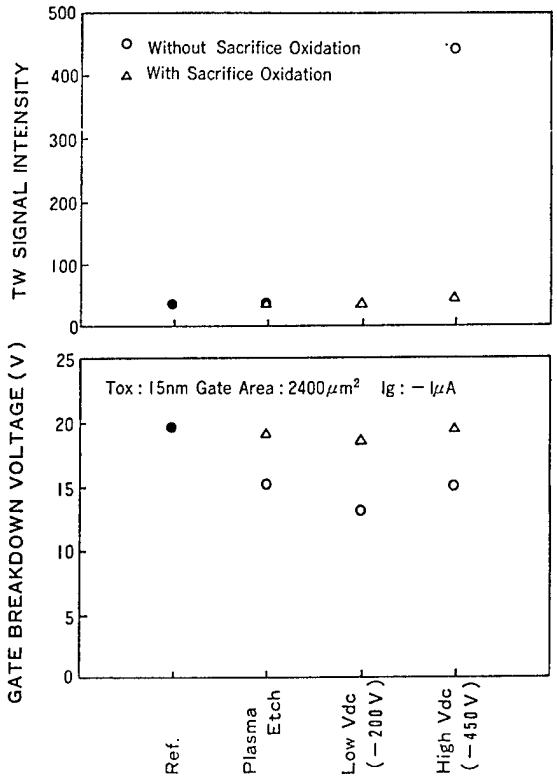


Figure 4. Values of thermal wave measurements under various etching conditions, and gate breakdown voltage.

In the case of plasma etching, the extent of damage is very small even after the etching, much the same as before that. In the case of silicon trench etching, however, damage is observed under both high and low bias voltage conditions. When oxidized film is removed through sacrifice oxidation at 800-1,000°C, however, it is found that the damage is removed from the silicon surfaces. Furthermore, we formed a 15nm thermally oxidized film on each of these surfaces, and producing a capacitor structure we investigated the breakdown voltage of the silicon oxide film formed on the silicon surface. From this breakdown voltage evaluation, too, we found that sacrifice oxidation causes the damage to be put into the SiO_2 formed, and that such oxidation, accomplished only once, makes it possible to remove the damage no matter what kind of etching process is used, and this can also be applied to devices.

Two factors are thought to bring about damage immediately after etching: surface contamination due to etching and the occurrence of a crystal defect on a silicon surface due to a collision between ions. The results of our XPS analysis of a silicon surface immediately after etching are given in Figures 5 and 6.

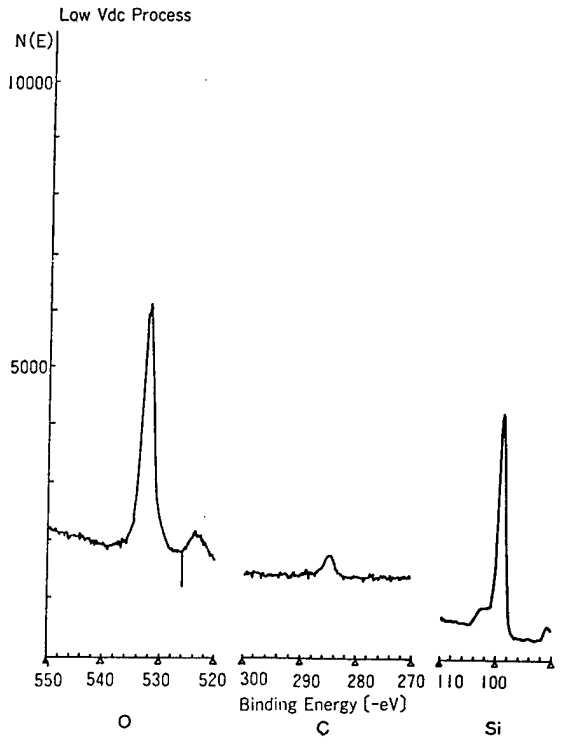


Figure 5. XPS evaluation of silicon surface under low bias voltage.

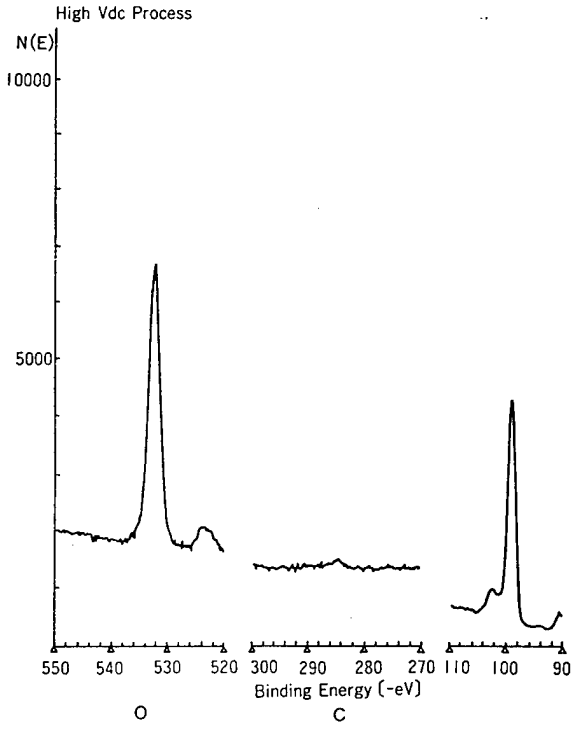


Figure 6. XPS evaluation of silicon surface under high bias voltage.

Under the condition of low bias voltage (in Figure 5), some carbon (C) was detected, but under the condition of high bias voltage (in Figure 6), where damage was found to be conspicuous, no peak connected with impurities was detected and the silicon surface was observed to be very clean. From these results, it can be assumed that the damage detected by the thermal wave method was not a surface contamination due to etching but was caused by colliding ions to the crystal structure of the silicon surface.

Figure 7 shows the result of our examination of transistor gain constants conducted by forming an MOS transistor on an etched surface.

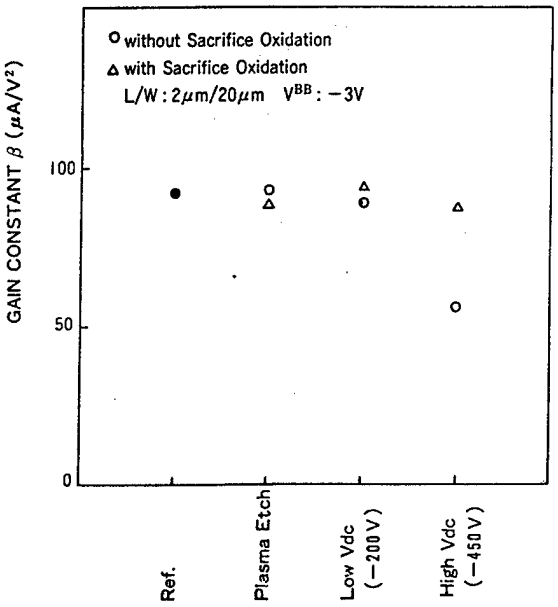


Figure 7. Transistor gain constants under various etching conditions.

Gain constants fall by only about 30 percent when an MOS transistor is formed on a silicon surface etched under high bias voltage conditions, showing a good agreement with the evaluation by the thermal wave method. Since great damage is thus left on the silicon surface, it is necessary to carry out sacrifice oxidation when this process is to be applied to devices. As can be seen from this, measures to reduce damage will have to be taken in the future. Figure 8 shows the result of our examination of junction leakage current, conducted by forming an n^+ area after arranging about 7×10^4 LOCOS areas, each measuring $3 \times 3 \mu m^2$, in a $1.7 \times 1.9 mm^2$ active area and etching the exposed silicon surface.

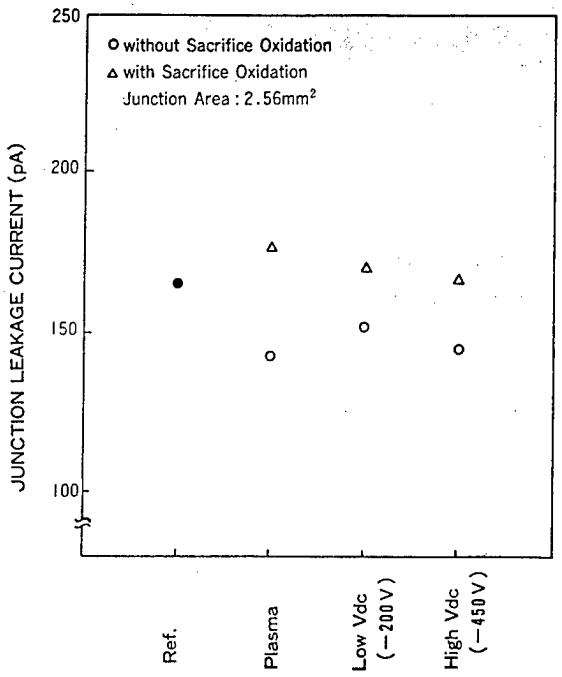


Figure 8. Junction leakage current under various etching conditions.

The leak current showed a favorable value of about 160pA regardless of sacrifice oxidation. It is conceivable that this silicon trench etching does not cause any damage to the terminal part of the LOCOS oxide film and the silicon substrate, or that it makes it possible to remove damage through heat treatment during the formation of the n+ area.

That is our evaluation of damage on an etched silicon surface. Figure 9 shows the result of our examination of breakdown voltage distribution of gate insulation film, conducted by forming a 1.2μm trench with a depth of 3μm on a silicon surface and performing sacrifice oxidation, followed by the creation of an $SiO_2/Si_3N_4/SiO_2$ three-layer gate insulation film, and creating an electrode on the insulation film with polycrystalline silicon.

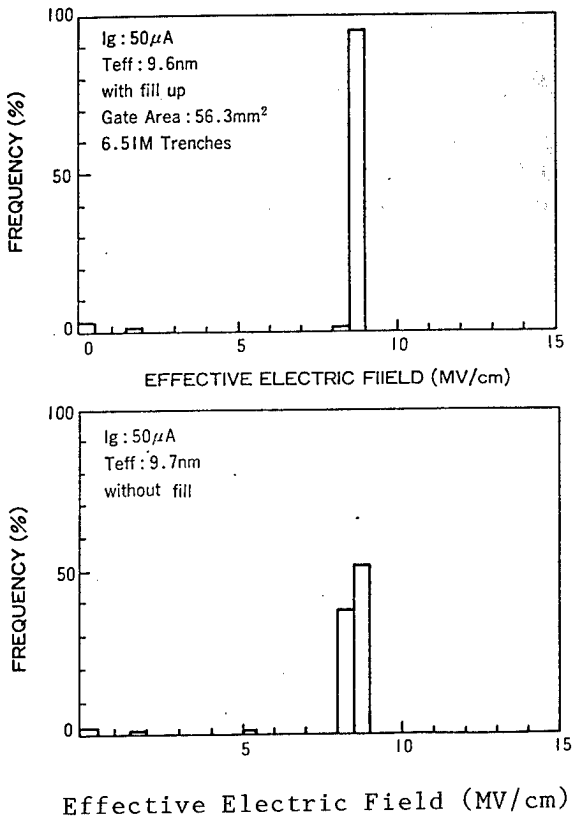


Figure 9. Gate breakdown voltage distribution in insulation film formed in a trench.

The upper part of the illustration shows a case where the trench is completely padded with insulation film, while in the lower part only the polycrystalline silicon electrode is formed, and the trench is hollow. In the case of giving positive voltage to the polycrystalline silicon electrode, even a gate insulation film that is as thin as t_{eff}=9.6nm exhibits a favorable breakdown voltage distribution, indicating that it can be fully applied to devices.

5. Conclusion

We found that in obtaining a trench profile with a high aspect ratio, it is advisable to carry out etching under the conditions of low pressure and high bias voltage. These conditions make it possible to change the profile and etching speed through a simple change in the ratio of gas composition, and also to hold down the dependence of the etching area as well as of the etching size to a low level. It can therefore be said that this is a favorable etching process. However, because of the great damage expected right after etching, sacrifice oxidation is necessary.

With further progress in integration expected in the future, etching processes will be required that cause still lower damage even right

after etching. Therefore, we consider it highly possible that the etching methodology itself will change.

Anticorrosion Measures

43064069 Tokyo SEMICON NEWS in Japanese Oct 88 pp 44-49

[Report by Yukimasa Yoshida, IC Process Engineering Department, Toshiba Corp.: "Aftercorrosion of Aluminum Alloys"]

[Text] Introduction

The enhancement of LSI integration has been making steady progress year after year. In the case of DRAM, for example, while the supply shortage of 1M DRAM's is posing a problem and the delay in the start of mass-production is being pointed out, shipments of 4M DRAM samples are reportedly underway. The integration of LSI is to be enhanced by reducing the size of the elements that constitute LSI.

The reduction of pattern size largely depends upon the progress in processing technologies, i.e., lithographic and etching technologies. With the design rule for the 4M DRAM standing at under 1μm, the age of submicron devices has dawned at last.

With the progress in fine patterning, maintaining and improving the reliability of devices will become more and more important. In the case of wiring materials, in particular, it is essential to take measures against electromigration and stress migration when the pattern size becomes 1μm or so. Therefore, materials laminated with Al-Si-Cu or with barrier metals are being adopted in place of the conventional Al-Si.

For the processing of Al alloys, a dry etching process using Cl gas is being adopted. To prevent Al wiring corrosion from occurring after etching (aftercorrosion), various kinds of aftertreatment are performed.

This corrosion is occurring more and more frequently with the use of new wiring materials. There has been no means of quantitatively ascertaining what kind of afterprocessing method is most effective and to what extent Al alloys should be processed.

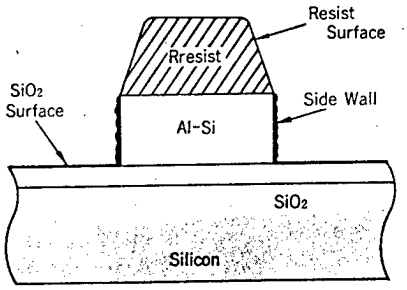
In this report I will dwell upon the Cl distribution on a wafer, the amount of Cl that remains on the wafer, the frequency of corrosion, and the effects of various kinds of postetching treatment, by using methods for quantitatively evaluating the amount of Cl sticking to a wafer.

Anisotropic Etching of Al Alloys

In the formation of fine patterns, the difference in transformation by etching should be narrowed as much as possible, and therefore it is essential to effect anisotropic etching without any undercut. The

mechanism to obtain anisotropic etching forms was examined some time ago, and the effect of protecting side-walls is found to be indispensable for Al alloys.

The side-wall protecting effect is a phenomenon whereby a film, consisting of a substance produced through photoresist resolution or reaction, is made to stick to a pattern side-wall in order to prevent the attack of Cl atoms or radicals, as shown in Figure 1.



Note: Anisotropic etching of the Al alloy is achieved through protection of the side-wall.

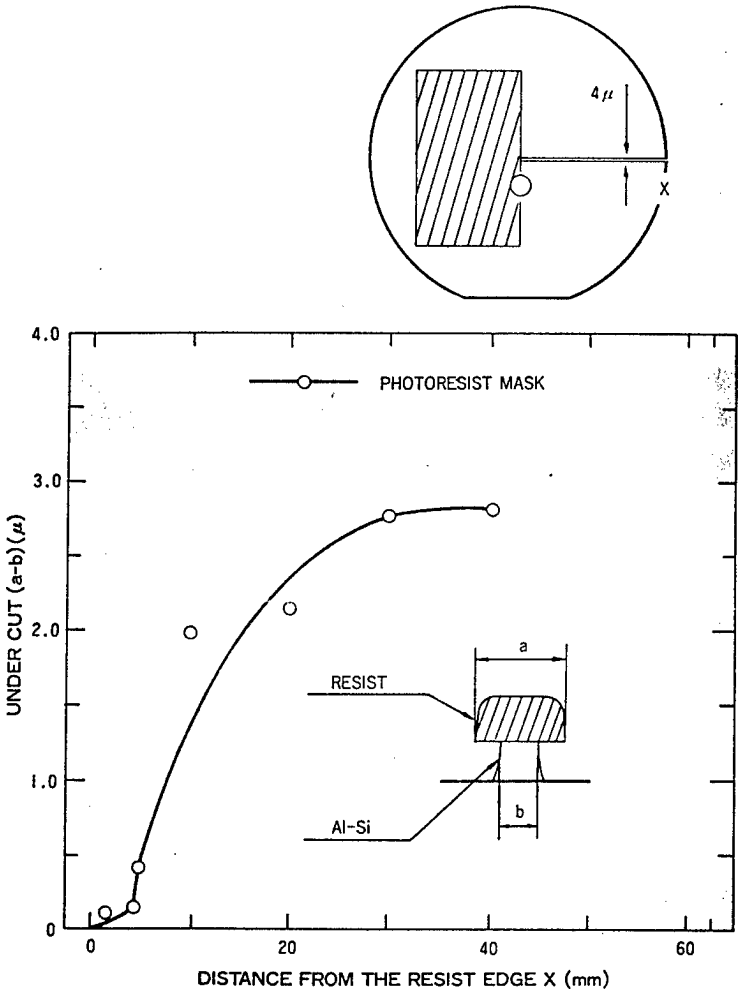
Figure 1. Cross-section of processed Al alloy.

Figure 2 [on following page] shows an experimental result revealing that the presence of a resist plays an important role in the form of the object to be processed by etching. The extent of undercut (a-b) increases with the distance from the resist edge.

Aftercorrosion and Aftertreatment

The Cl_2 or the reactive product ($AlCl_3$) that sticks to a wafer during the etching process is highly moisture-absorbent and produces HCl through its reaction with the moisture in the air. The surface of an Al pattern produced immediately after etching is covered with oxidized film (Al_2O_3) or protective film, but corrosion caused by the HCl spreads from a place where the oxidized film or the protective film is insufficient. Therefore, various methods for aftertreatment are being devised to remove the Cl-containing substance on the wafer.

These methods include exposing the wafer to F-system gas plasma after etching so that the remaining Cl is replaced by F, taking out the resist to the air after exfoliating it, oxidizing the substance at low temperature and covering the surface with Al_2O_3, heating it, washing it with water, etc. However, to determine what method is the most effective or to what extent such measures should be taken, it is necessary to ascertain quantitatively the amount of Cl sticking to the wafer.



Note: The extent of undercut increases in proportion to its distance from the edge (the circle in the illustration) of the part (▨) covered with the resist on the wafer.

Figure 2. Effects of resist on Al-Si processing.

Ion Chromatography for Evaluation of Cl Sticking to Wafer

The amount of Cl that remains sticking to a wafer can be evaluated by ion chromatography, which is widely used to measure the density of ions in a solution.

A wafer is dipped in a given amount of pure water (50ml in this case) and left there for a specific time. The Cl or compound containing Cl adsorbed on the wafer dissolves in the pure water. The extent of its adherence to the wafer can be ascertained by measuring the density of Cl ions in the pure water by ion chromatography. My examinations of Cl distribution on a wafer are as follows.

Most Cl Remaining After Etching Sticks to Side-Walls of Al Patterns

When a dry etching process is adopted to form Al wiring through use of a Cl-system gas, Cl remains on the wafer. I carried out examinations to see on what part (as shown in Figure 1) the residual Cl was adhering--whether it was sticking to the resist surface, SiO_2 or the side-wall of the Al pattern. After etching the five kinds of sample wafers shown in Figure 3 [on following page], I measured the amount of the residual Cl by ion chromatography. Wafers 1 and 2 were used to obtain the amount of a gas sticking to the resist and to SiO_2, respectively, during the etching process; wafer 3 to obtain the amount of a gas sticking to an SiO_2 substrate film after Al-Si etching; and wafer 4 to obtain the amounts of a gas and a reactive product sticking to the resist during the etching process. Using the values obtained, on the basis of hypothesis, I classified the amount of adhesion in the case of wafer 5 (pattern consisting of line and space 2μm wide).

First I found that, with an Al wired pattern, Cl remained in a large amount, as shown in Table 1, and it stuck to SiO_2 very slightly.

Table 1. Cl Amounts Recognized in Respective Samples (ppb)

Sample No.	Cl-Ion Concentration
1	105
2	6
3	150
4	245
5	1140

Next I calculated the areas of the resist, the SiO_2 and the side-wall of the Al pattern in wafers 1-5, and classified the amounts of residual Cl. As a result, I found the greater part of the residual Cl sticking to the side-wall of the Al pattern, as shown in Figure 4.

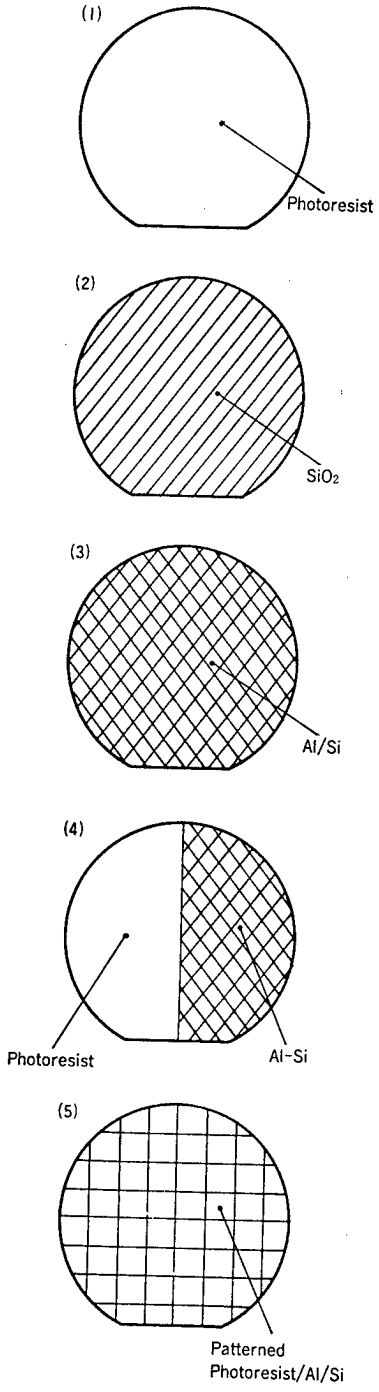


Figure 3. Sample wafers.

Note: 1. Entire surface coated with resist
2. SiO_2
3. Al-Si put on SiO_2
4. Half area of Al-Si film coated with resist
5. Pattern consisting of 2μm-wide line/space

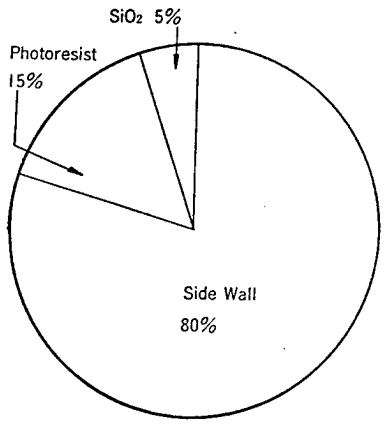


Figure 4. Classification of amount of Cl sticking to wafer.

This means that a large amount of Cl is contained in the side-wall protecting film of the Al pattern. It is conceivable that the aftercorrosion is caused by this Cl.

Reducing Amount of Cl by Postetching Treatment

The effects of the postetching treatment designed to prevent aftercorrosion were evaluated on the basis of the amount of residual Cl. Here they are compared as to the processes of wafer heating, N_2 blow and washing with water.

Figure 5 [on following page] shows the results of measuring the amount of residual Cl after heating the postetching wafer on a hot plate.

When no treatment is given, the amount is a high value of 1,600ppb, but it drops as a result of wafer heating. The extent of the drop largely depends upon the heating temperature. In light of the fact that the vapor pressure of $AlCl_3$ changes markedly in this range of temperature (1Torr at 100°C rises to about 760Torr in atmospheric pressure at 180°C), it is assumed that the greater part of the residual Cl on the wafer consists of $AlCl_3$ that is produced through etching reaction.

Figure 6 [following Figure 5] shows the effects of N_2 blow treatment. In this case, it does not largely depend upon temperature, and no difference due to flow is observed in this range.

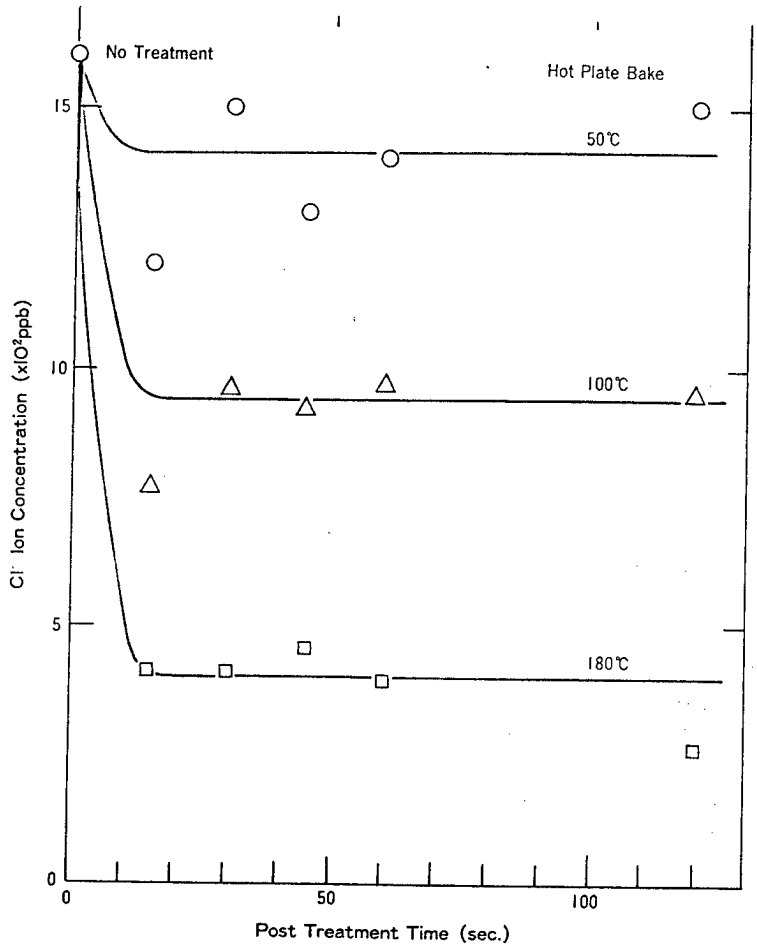


Figure 5. Effects of Cl removal with hot plate (largely dependent upon temperature).

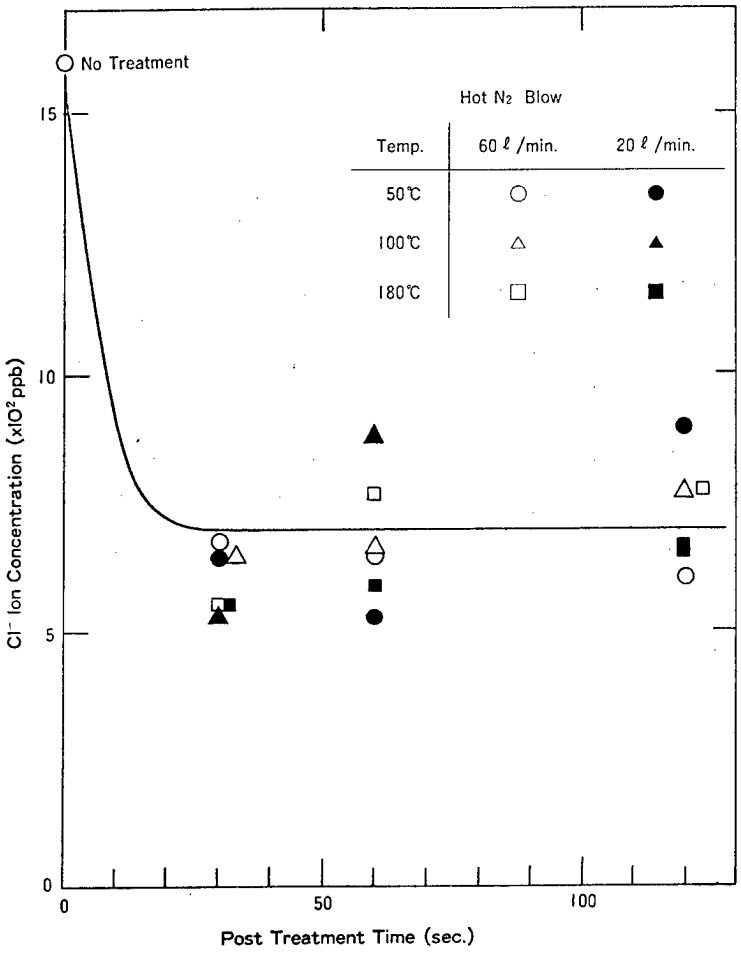


Figure 6. Effects of Cl removal by N_2 blow.

Figure 7 [on following page] shows the effects of Cl removal through rinsing with pure water.

Compared with the aforesaid two methods, the amount of residual Cl is reduced to the largest extent by this method. If washing with water is performed right after etching, however, high-density HCl comes into being instantaneously and threatens to cause Al corrosion. Therefore, initially removing most Cl by heat treatment and then carrying out a flushing process is thought to be most effective.

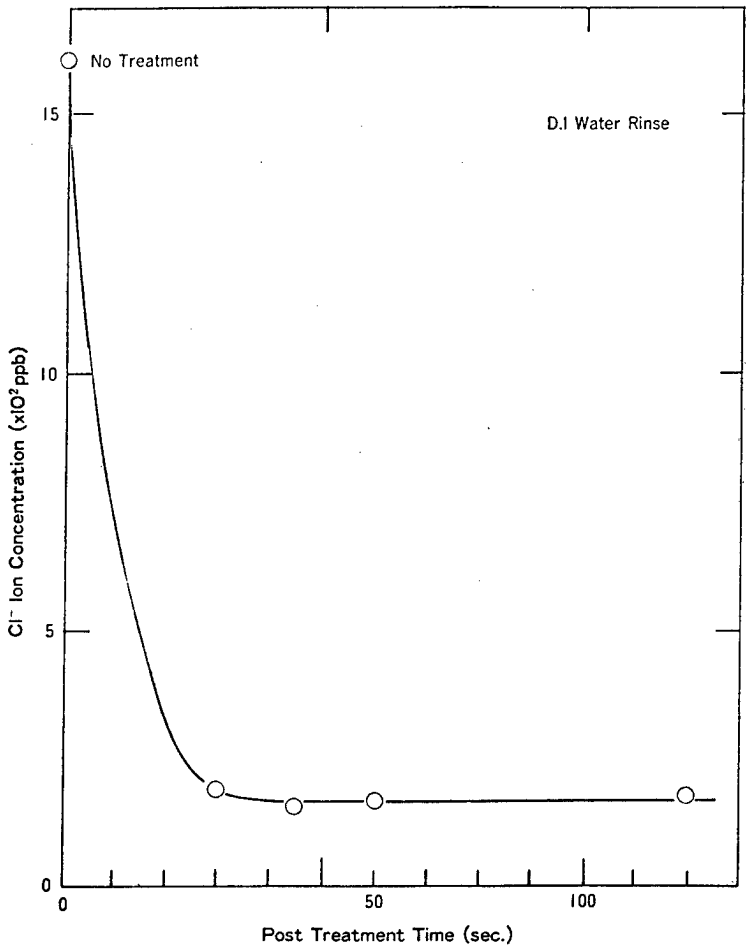


Figure 7. Effects of Cl removal through rinsing with pure water (largest amount of removal).

Amount of Residual Cl and Frequency of Corrosion

It was found possible to measure the amount of residual Cl on a wafer by ion chromatography and to compare the effects of various postetching processes. Therefore, I next examined the relationship between the amount of residual Cl and the frequency of corrosion.

Figure 8 shows the result of calculating the frequency of corrosion with an optical microscope, by changing the amount of residual Cl on a wafer under different postetching conditions and leaving it for a week.

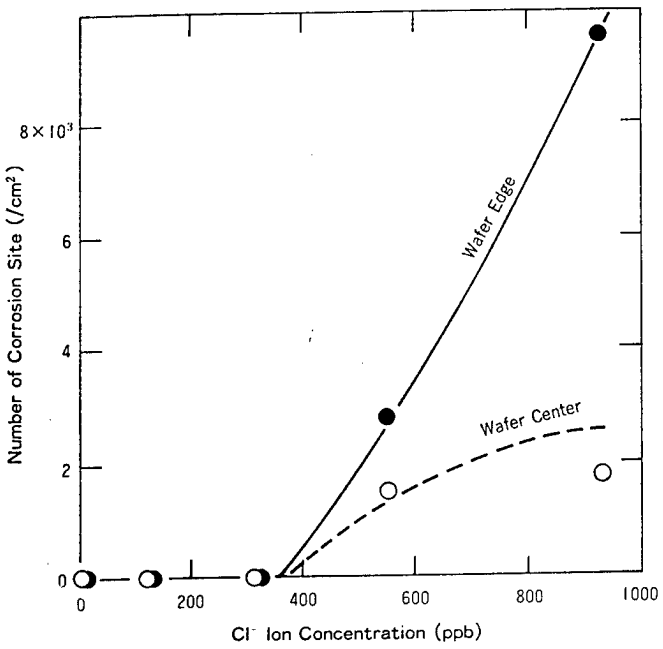


Figure 8. Amount of residual Cl and frequency of corrosion.

Corrosion occurs when the amount of residual Cl exceeds a certain threshold, resulting in an increase in the number of corrosion sites as well as in the amount of the residual Cl.

The occurrence of corrosion is more frequent near the periphery of a wafer than in its central part. The cause of this is not clear, but it is conceivably due to no uniformity of etching or film quality.

Figure 9 [on following page] shows the result of my examination of the relationship between the amount of residual Cl and the open yield of wiring 2μm wide and about 6m long, which was subjected to a disconnection test through electric measurement.

The result shows that the open yield declines from the neighborhood of the corrosion threshold, giving rise to wire disconnection.

Al-Si-Cu Tends To Bring About More Corrosion Than With Al-Si

I carried out a similar experiment with Al-Si-Cu. The number of corrosion sites showed an increase in comparison with Al-Si, but the size of the corrosion was smaller. Photos 1 and 2 [not reproduced] exhibit the appearance of corrosion in Al-Si and Al-Si-Cu, respectively. The extraneous substance protruding from the wiring is thought to be $Al(OH)_3$.

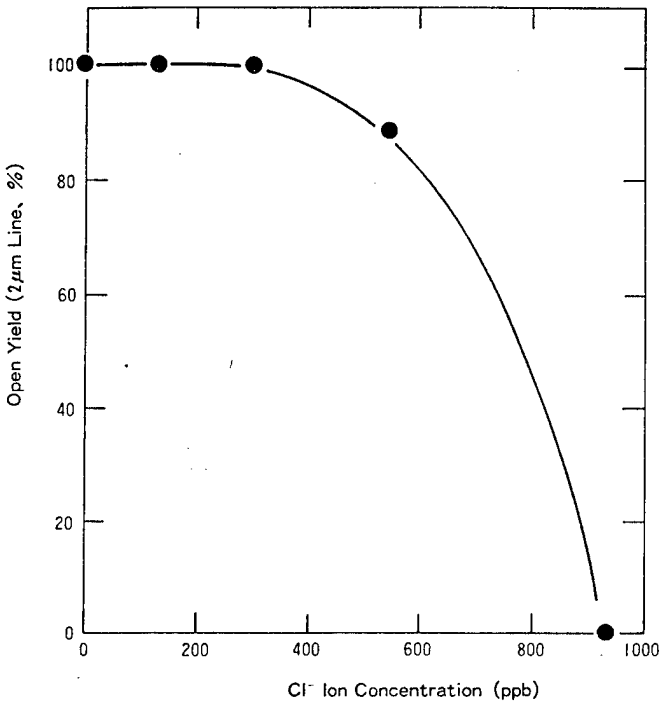


Figure 9. Amount of residual Cl and electric open yield (compared with the corrosion checked by an optical microscope, observable in Figure 8, a poor open yield originates from the same level).

The difference in the size of corrosion between Al-Si and Al-Si-Cu is conceivably due to the difference in grain size. It is also thought that corrosion occurs more often in Al-Si-Cu because of the electrolytic corrosion (galvanic corrosion) arising when extraneous metals (Al and Cu) are present.

Conclusion

Various alloys and laminate substances are being investigated as wiring materials for LSI's. In comparing them from the viewpoint of reliability, tolerance to corrosion as well as to electromigration and stress migration is an important factor.

Many kinds of aftertreatment are given for the purpose of preventing aftercorrosion caused by etching, but it has become possible to evaluate their effects quantitatively by the methods described in this report. With regard to the mechanism causing corrosion, there are many points that should be elucidated, and the same methods are effective for this purpose, too.

Photo Resist Removal Technology

43064069 Tokyo SEMICON NEWS in Japanese Oct 88 pp 50-54

[Report by Shuzo Fujimura, Keisuke Shinagawa, Junichi Konno, and Hiroshi Yano, Process Development Department, Semiconductor Business Headquarters, Fujitsu, Ltd.]

[Text] Introduction

Resist removal is a somewhat exceptional etching process. Since the resist must become completely (?) nonexistent after the ashing process, there is no stage for any primary value judgment on such matters as the form of a cross-section after etching or a selective ratio to the mask. This is very different from an etching process wherein it is possible to judge right afterward whether it has been satisfactory or not. It may be possible to form a judgment as to whether a resiuum occurs or the substrate becomes defective, but only in the case of removing a resist after ion injection or a specific etching process, and not in ordinary cases of resist removal. After all, whether the ashing process is satisfactory depends largely upon the change in the property of the device in terms of "damage." Since damage also depends greatly upon the device structure, comprehensive knowledge of the device structure and device manufacture is necessary in order to develop the resist removing process. From this point of view, those in charge of development among device makers need to make great efforts. However, if attention is paid to the basics, first of all, it will be possible to form fairly accurate estimates about damage. We will therefore sum up the basic matters regarding damage, to begin with.

1. Damage

There are three main types of damage that occur at the time of resist removal that are commonly recognized: gate breakdown due to plasma density, contamination by movable ions (Na in a concrete term) from the resist, and contamination by a heavy metal from the resist. In addition, contamination by hydrogen or carbon has also been pointed out, but there are still many unclear points requiring study on the extent of damage and possibilities of recovery, and it is impossible to ascertain fully the actual state of damage. Therefore, we think it is not yet time to carry out concrete studies on measures to cope with it.

The problem of gate breakdown due to plasma density shows that in the case of processing a wafer in plasma, it is necessary not only to make the processing uniform but also to improve the distribution of plasma itself. Therefore, the method of securing the uniformity of processing by moving a wafer or plasma has come to be in doubt as to its effectiveness. From the viewpoint of uniformity of plasma, RF with waves longer than microwaves, having much the same length as the wafer size, is thought to be suitable for plasma excitation in the case of

processing a wafer in plasma (though this is not applicable when ECR discharge is used). In other words, this problem has placed a big restriction on the structure of equipment for wafer processing in plasma.

Contamination due to Na from the resist has long been recognized, and therefore many reports have been made on it. This contamination can be detected in a simple way and with high sensitivity by measuring a flat band shift after BT processing. Therefore, this method is almost always used in evaluating the resist removing process. It is known that contamination due to Na is eliminated through high-temperature annealing. Except in a very serious case of contamination, it is inadvisable to evaluate an asher, for example, on the basis of an overly small difference in ΔVfb value. In such countries as the United States, this is said to pose a problem in a process after Al wiring where a high-temperature annealing process cannot be used. We wonder what Japanese semiconductor manufacturers think about this? Anyhow, this is a convenient evaluation parameter to use as a means of declining an offer of equipment that they do not want to buy.

As for the third kind of damage, contamination due to a heavy metal from the resist, such a metal shortens the life of a small number of carriers, and therefore this contamination is an especially serious problem for MOS DRAM's, etc. Moreover, no effective method for recovery has been found for the present. Consequently, we think that this is the most important problem. Figure 1 shows the result of our examination of the permeability of Si oxide film contaminated by a heavy metal, conducted by using a highly sensitive tester.

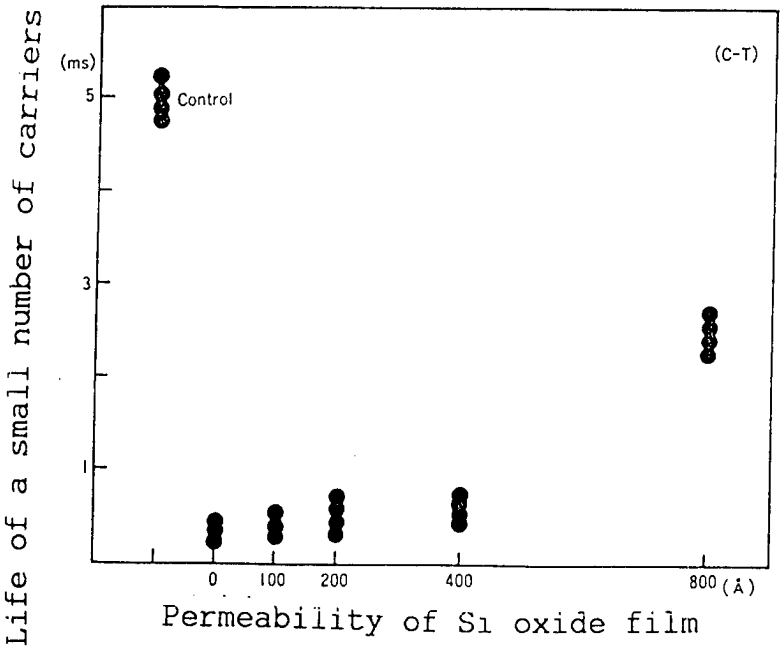


Figure 1. Permeability of Si oxide film contaminated by a heavy metal from the resist.

Surprisingly, plasma ashing causes a heavy metal to pass readily through the gate oxide film of currently used MOS devices. In the future, oxide film is expected to become thinner and devices are also certain to become more sensitive; therefore, this problem is expected to become increasingly serious. This contamination by a heavy metal from the resist occurs in the manner shown in Figure 2. Here the heavy metal is led to a device through a collision between the heat in the plasma and charged particles.

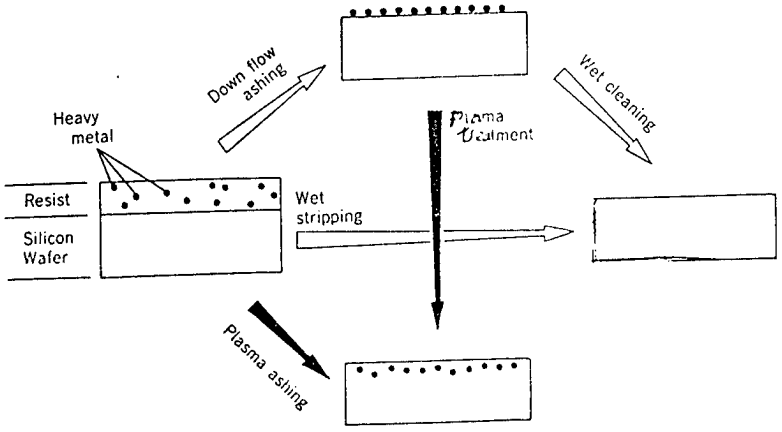


Figure 2. Occurrence of contamination by heavy metal from resist.

As for the effects of heat, contamination occurs at a level at which it can be easily detected when the temperature is not less than 300°C, as shown in Table 1.

Table 1. Heat Effects on Contamination by Heavy Metal

300°C	Resist + 300°C	400°C	Resist + 400°C
$542_{\sigma=32}$	$416_{\sigma=43}$	$537_{\sigma=18}$	$488_{\sigma=36}$

μsec

We cannot say anything about temperatures below 300°C, because there are no definite data available. However, we would like to lower the ashing temperature to less than 200°C, or less than 150°C if possible, close to the post bake temperature. Of course, we do not want to use halogen, because the lower layer should not be etched.

On the other hand, there is as yet no criterion for quantitative judgment of the effects of charged particles. The relationships between contamination and the plasma parameters of electron density, ion implantation energy, etc., have not yet been ascertained. In some cases, advantage has been taken of this point by advertising equipment, having a process close to plasma, as a damage-free downflow asher. As

downflow and downstream are terms representing the downstream of plasma, it may be possible to call it "downstream equipment" if there is a wafer on the exhaust side from the plasma or a plasma shield between the plasma and the wafer. However, this equipment is so small that the effect of charged particles can be ignored, and therefore it is different from a "downflow process" that is regarded as capable of fulfilling most cases of chemical ashing. Therefore, we hope that equipment manufacturers will label equipment that is capable of a "downflow process" as "downflow equipment." (When activation energy is about 0.5eV in the case of ashing a novolac resin resist by using only O_2 for convenience sake, we set up a criterion for such cases in terms of a "downflow process.")

It can be concluded that the resist removing process required in the case of the above-mentioned three kinds of damage should be an ashing process that makes it possible to ignore the effect of charged particles at a temperature of less than 150°C or so. However, the problem is that this will not remove the resist after ion implantation.

2. Resist Removal After Ion Implantation

After ion implantation the resist can be grouped into three layers from the surface--a cross-contaminated layer, a carbonized layer and an unchanged layer (Figure 3).

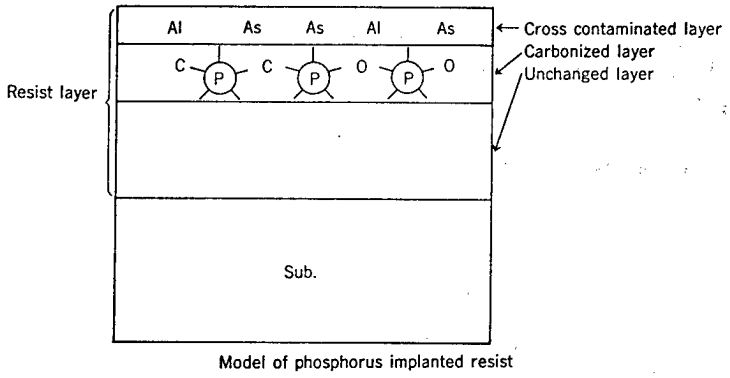


Figure 3. Resist structure after high-dose ion implantation.

It is known that the presence of residue after the removal of oxygen plasma is due to an impurity in the cross-contaminated layer as well as to a dopant in the carbonized layer. Most residue components consist of a mixture of dopant oxide and carbon, and therefore they can be removed almost completely when hydrogen plasma is used. Is it not possible to remove them chemically?

Figure 4 shows the structure of a carbonized layer formed in novolac resin into which a large amount of phosphorus is implanted.

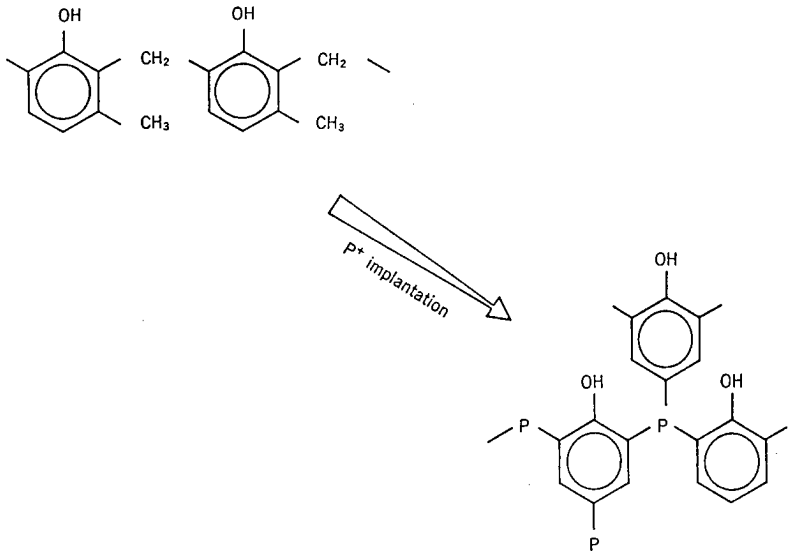


Figure 4. Carbonized layer of resist formed in phosphorus implanted novolac resin.

The phosphorus crosslinks the novolac resin and is also surrounded by a benzene ring. A method of chemically resolving such a structure is not yet known. What is necessary to remove it for the present is to cause, for instance, a collision of charged particles, which would destroy this structure in a physical way. Moreover, a structure containing many benzene rings is known to be resistant to the impact of ions or the like. Therefore, if the energy for the implantation of charged particles and the amount of implantation are reduced for the purpose of avoiding damage, it will become more and more difficult to remove the resist. It is therefore unavoidable to use plasma in a region where degraded layers are to be removed.

To what extent should ion implantation be carried out before use of the smallest possible amount of plasma becomes necessary? Figure 5 shows changes in the film thickness of a novolac resin resist, as against the amount of ion implantation. It reveals a sharp decrease in film thickness from $10^{14}/cm^2$ to $10^{15}/cm^2$.

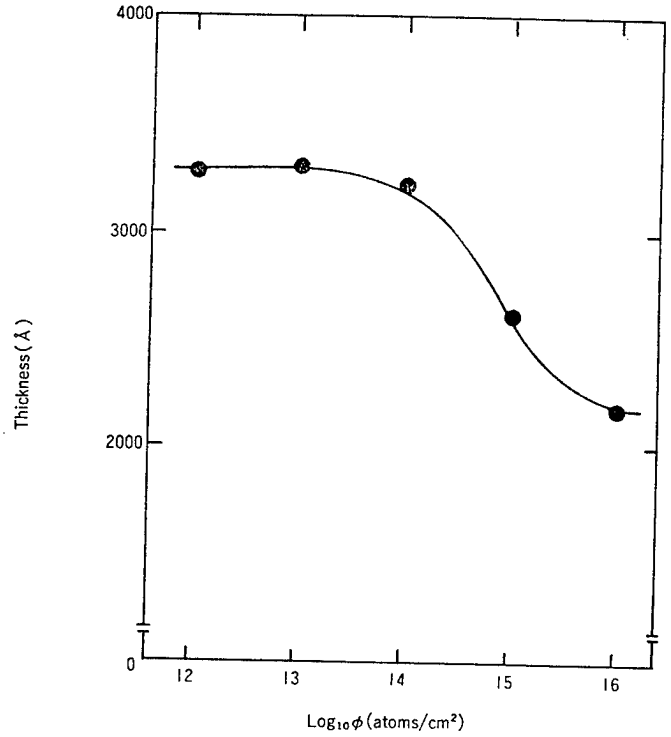


Figure 5. Changes in film thickness of novolac resign resist, as against amount of ion (P^+) implantation (70keV).

Figure 6 shows the dependence of the amount of ashing in O_2 + CF_4 downflow upon the dose.

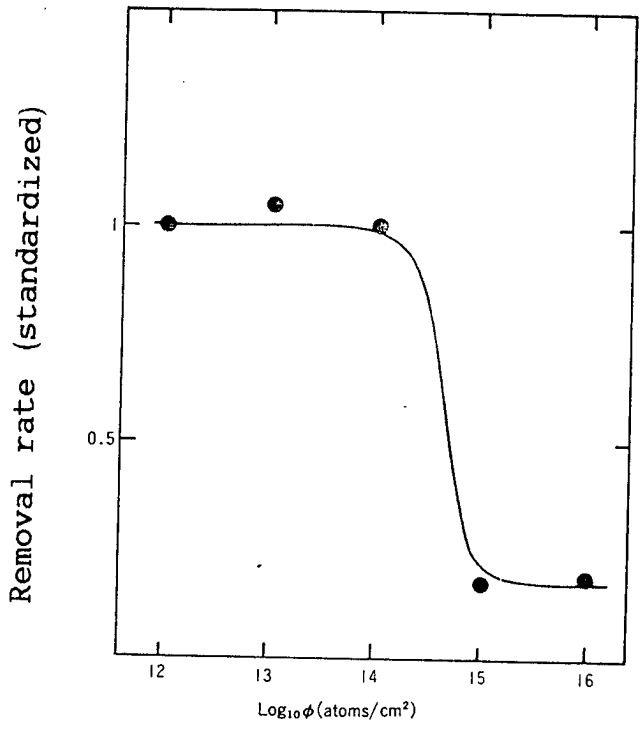


Figure 6. Ashing rate in O_2+CF_4 downflow of novolac resin resist to the amount of ion (P^+) implantation.

Likewise, the rate falls markedly from $10^{14}/cm^2$ to $10^{15}/cm^2$. From these facts, it can be assumed that in the case of ion implantation above $10^{15}/cm^2$ or so, the resist structure changes to some extent when phosphorus is used. Therefore, when a change in resist structure is observed by using solid NMR, SP^2/SP^3 is found to become lowest in the case of $10^{15}/cm^2$, and to increase gradually when the dose is a larger amount (Figure 7).

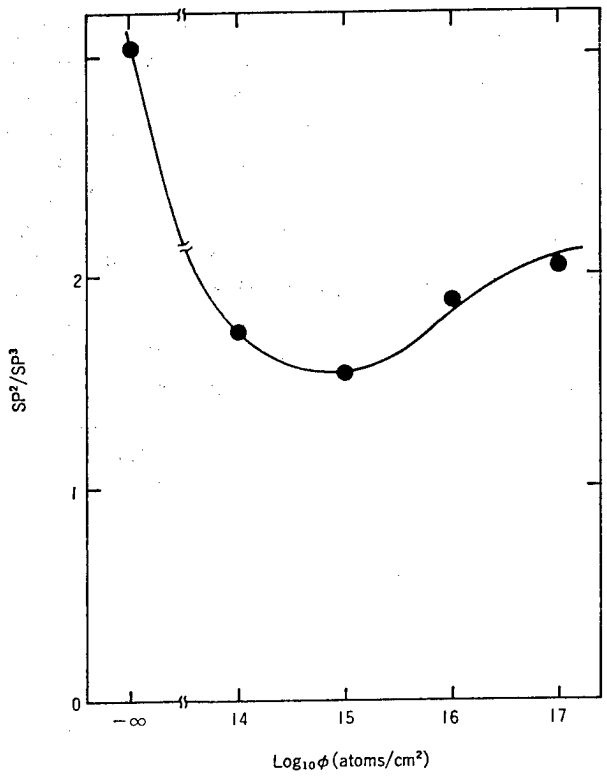


Figure 7. Change in carbonized layer structure of novolac resin resist, compared with amount of ion (P^+) implantation.

This means that a new SP^2 is created, i.e., that a new double coupling and a benzene ring arise at the dose limit of about $10^{15}/cm^2$. In other words, when phosphorus is injected, a degraded layer is formed with a dose of more than $10^{15}/cm^2$, and plasma or the like becomes necessary to remove it.

So far we have described conditions requiring direct resist processing in plasma after ion implantation and we have made the point that plasma, consisting mainly of hydrogen rather than oxygen, is effective in removing degraded layers. Prospects have also been obtained for determining the restrictions imposed by damage on processes. Therefore, the remaining task is how to make process designs in coordination with actual devices. This depends upon the abilities of those engaged in the

development of processes or equipment, and so we will not express any opinions about that here.

Conclusion

In this report we have stated our views on the restrictions on processes that will be required in the future, paying attention to two problems in the development of resist removal technology--damage and post-ion implantation resist. There will not be many cases where all requirements in this connection must be filled. These requirements include, for example, measures to be taken after covering gate oxide film with a resist and implanting ions to the peripheral region. An ordinary resist removing process can be fully carried out even in a slightly rough way of removal. In other words, it is important to make proper use of any removing process. We think it is not wise to make do with a single process simply because the object of etching is a resist. The etching equipment, for example, should be appropriate for the purpose. Equipment having specific characteristics, such as causing little damage in spite of a somewhat poor throughput, or removing the resist completely after high-dose ion implantation but at a high price, will probably be easy to use in the future. In any case, the process parameters must be measured correctly and with high reliability as a prior step. In other words, if the temperature of a wafer, the power of μ waves, etc., are not measured correctly, there will be no way of making proper use of the processes. In this regard, we think it is inevitable that the cost of equipment will increase to some extent.

Device Applications for Superconducting Thin Films

Multilayer SQUID

43067071 Tokyo THE 49TH AUTUMN MEETING OF THE JAPAN SOCIETY OF APPLIED PHYSICS (ABSTRACTS) No 1 in Japanese 4-7 Oct 88 p 114

[Article by Hideaki Nakane, Toshiyuki Aida and Ushio Kawabe, Central Research Laboratory, Hitachi, Ltd.: "Multilayer SQUID With High Tc Oxide Superconductor Films"]

[Text] Preface. The use of high-temperature superconductor $YB_2Cu_3O_{7-6}$ thin films makes it possible to manufacture superconducting devices that operate in liquid nitrogen.[1,2] Hitachi has previously mounted a SQUID and an input coil, respectively, on different substrates and connected the substrates to each other in layers to manufacture a superconducting device.[3] Now, however, Hitachi has manufactured a device in which a SQUID and an input coil are mounted in layers on the same substrate, and has studied the performance of the device.

Experiments and Study. A $YBa_2Cu_3O_{7-6}$ thin film formed by the RF magnetron sputtering method was processed in the shape of a SQUID using photolithography and chemical etching methods. Next, an interlayer insulating MgO film was put on the SQUID in layers. In this case, a contact hole was provided to connect an input coil. Finally, an Er $Ba_2Cu_3O_{7-6}$ thin film was applied in layers to serve as a superconducting thin film for the input coil, and was processed in a coil pattern. Thus, a multilayer SQUID was prepared. The I-V characteristics and V-ϕ characteristics were confirmed at 4.2K. A comparison of the V-ϕ characteristics cycle (with respect to magnetic flux) of the new device with that of previous devices revealed that the coefficient of connection of an input coil to a SQUID is improved by about 3.4 times. This appears to be the result of the decrease in the interlayer insulating film thickness.

References

1. H. Nakane, et al: Jpn. J.A.P. 26, L1581 (1987)

2. H. Nakane, et al: Jpn. J.A.P. 26, L1925 (1987)

3. H. Nakane, et al: Springtime Applied Physics preliminary draft p. 107 (1988)

Thin Film Device Processing

43067071 Tokyo THE 49TH AUTUMN MEETING OF THE JAPAN SOCIETY OF APPLIED PHYSICS (ABSTRACTS) No 1 in Japanese 4-7 Oct 88 p 114-115

[Article by Koichi Mizuno, Michihiro Miyauchi, Kentaro Setsune and Kiyotaka Wasa, Central Research Laboratory, Matsushita Electric Co., Ltd.: "Process for Low-Temperature Synthesized Oxide Superconducting Thin Film Devices: Superconductivity of Oxide Superconductor Prepared on GaAs/CaF Substrate"]

[Text] Preface. We put a CaF_2 buffer layer on a GaAs substrate, on which we prepared a YBCO thin film. Thus, we confirmed the characteristics of oxide superconducting thin film devices. This report outlines the results.

Process. A semi-insulating GaAs (100) substrate was used. The CaF_2 buffer layer was deposited to a thickness of 200 nm by the vacuum evaporation method. A YBCO thin film was prepared to a thickness of 200 to 300 nm at 0.4Pa ($Ar:O_2$ = 2 : 1) and a charged power of about 130W using the rf magnetron sputtering method. The goal of the experiment was to prepare a powder having a composition ratio of 1 : 2 : 4.5. The substrate temperatures during film preparation were monitored by an infrared radiation thermometer and an alumelchromel thermocouple.

Results. The characteristics of the film thus obtained varied greatly depending on substrate temperature. However, critical temperatures of Tc_{on} = 75K and Tc_{end} = 45K were obtained at a substrate temperature of 450°C (Figure 1). The critical current density (Jc) was estimated to be 2×10^3 A/cm^2 at 4.2K. At substrate temperatures exceeding 4.2K, the YBCO film exfoliated. The X-ray diffraction pattern of the YBCO thin film shows that a slight peak believed to be Cu (111) appeared at about 44°C and that no layer-shaped Perovskite structure (generally observed) peaks appeared (Figure 2). In view of the fact that the current density is small, it is thought that the superconducting current flows along a path of microscopic crystals. The details, however, are being studied.

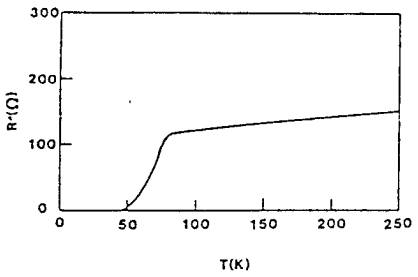


Figure 1. Resistance Transition Curve

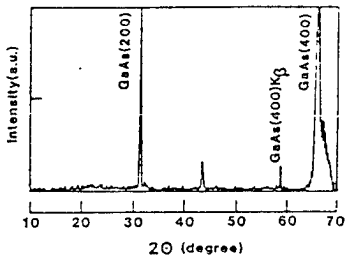


Figure 2. X-Ray Diffraction Pattern

$LiNbo_3$ Film Substrate

43067071 Tokyo THE 49TH AUTUMN MEETING OF THE JAPAN SOCIETY OF APPLIED PHYSICS (ABSTRACTS) No 1 in Japanese 4-7 Oct 88 p 114

[Article by Akira Enokihara, Koichi Mizuno, Hidetaka Higashino, Shigemi Kohiki, Kentaro Setsune and Kiyotaka Wasa, Central Research Laboratory, Matsushita Electric Co., Ltd.: "Process for Low-Temperature Synthesized Oxide Superconducting Thin Film Devices: Electrical Properties of Superconducting Thin Films Prepared on LiNbO Crystals"]

[Text] The use of $LiNbO_3$ as a high-temperature superconducting thin film substrate is very important, because $LiNbO_3$ can potentially be applied to optical elements and surface acoustic wave elements. Therefore, we prepared a Gd-Ba-Cu-O thin film on $LiNbO_3$ crystals and investigated the electrical properties and the diffusion of atoms from the substrate into the film.

We formed a Gd-Ba-Cu-O thin film (having a thickness of 660 nm) on an optically ground z-cut $LiNbO_3$ crystal substrate at a substrate temperature of 600 °C using the high-frequency magnetron sputtering method. Figure 1 shows the relationship between film resistance and temperature, and Figure 2 shows the relationship between critical current density and temperature. The superconducting transition temperature and the on-set temperature were 48K and 92K, respectively. Further, the critical current density at 4.2K was 6.4 X $10^3 A/cm^2$. In order to investigate the amount of diffusion of atoms (existing in the substrate) into the film, the amount of Li and Nb present in the substrate was measured by the atomic absorption method. These atoms, however, were not detected in the film. It appears that the diffusion of atoms existing in the substrate into the Gd-Ba-Cu-O film has little effect when a thin film is prepared at low temperatures, i.e. about 600°C. It is necessary to study the optimization of thin film manufacturing conditions, practical application to devices, etc.

9.7Ghz, a (Shapiro) step was observed, as shown in Figure 2. It appears that clearer steps can be observed by making the gap portion of the film thinner and also by reducing the length.

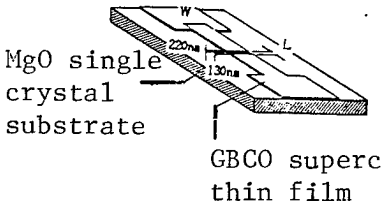


Figure 1. VTB Specimen

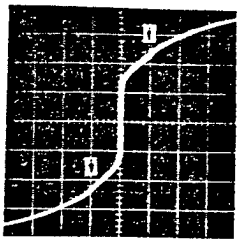


Figure 2. ↕I: 0.2 mA/div
9.7 GHz
↔V: 20 μm/div
4.2K

Protective Film Technology

43067071 Tokyo THE 49TH AUTUMN MEETING OF THE JAPAN SOCIETY OF APPLIED PHYSICS (ABSTRACTS) No 1 in Japanese 4-7 Oct 88 p 115

[Article by Takashi Hirao, Masotoshi Kitagawa, Takeshi Kamada, Shigenori Hayashi and Kiyotaka Wasa, Central Research Laboratory, Matsushita Electric Co., Ltd.: "Process for Low-Temperature Synthesized Oxide Superconducting Thin Film Devices"]

[Text] Preface. For the practical application of high-temperature superconducting thin films to electronic elements, it is essential to be able to form both extremely thin insulating films for tunnel junctions and passivation insulating films without damaging the superconducting thin films. We have studied an interaction between restorable components (arising from plasma decomposition) and superconducting thin films during the formation of insulating films by the ECR plasma CVD method and RF plasma CVD method using SiH_4.

Experiments. The interaction between an H_2 plasma and Gd-Ba-Cu-O thin films was investigated by XPS and the X-ray diffraction method at room temperature for the ECR plasma method and at 200°C for the RF plasma method, respectively. The element composition distribution after the formation of SiN insulating films was investigated by the AES method.

Results and studies. Figure 1 shows the dependence of Gd-Ba-Cu-O surface (having undergone H_2 plasma treatments) Cu XPS data on the process. The figure shows that restoration occurs more strongly in the

RF plasma method, compared to the ECR plasma method. Also, a change (c axis length) in the crystal structure was observed by the X-ray diffraction process when the RF plasma method was used. Meanwhile, the case of SiN film formation using SiH_4-N_2, no changes occurred in the crystal structure regardless of the methods used. We intend to study these interface reactions based on plasma spectrochemical data.

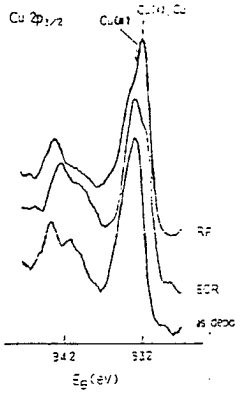


Figure 1. Dependence of XPS on Process

Grain Boundary Josephson Devices

43067071 Tokyo THE 49TH AUTUMN MEETING OF THE JAPAN SOCIETY OF APPLIED PHYSICS (ABSTRACTS) No 1 in Japanese 4-7 Oct 88 p 148

[Article by S-B. Ying, C-H. Park, Makoto Hatanaka, Toyohisa Yoshinari, Yuji Takeda, Tadayuki Kobayashi and Toshinari Goto, University of Electro-Communication: "Grain Boundary Josephson Devices Using Oxide Superconductor Thin Film"]

[Text] 1. Preface. High-temperature oxide superconductors composed of Y-Ea-Cu-O and Bi-Sr-Ca-Cu-O have been discovered. The creation of Josephson devices using these oxide superconductors will make it possible to operate SQUID's at high temperatures, detect electromagnetic waves, etc., thus serving to enlarge the range of practical applications for superconductors. It should be noted, however, that new devices equivalent to conventional metal group devices have not yet been obtained. Therefore, we have experimentally studied the possibility of manufacturing grain boundary Josephson devices.

2. Manufacture of devices. Y or Bi group films were formed on an MgO substrate by the RF sputtering method and the pattern shown in Figure 1 was formed by photolithography and chemical etching.

3. Results of measurements. Figure 2 shows the 9.67 GHz microwave response (at 4.2K) of a device manufactured using a YBCO film (having a thickness of 2 μm) annealed in O2 gas at 940°C. The lowest curve shows I-V characteristics when microwaves are absent. The upper side curves show stronger microwave emissions. Very satisfactory steps can be observed, which indicate that a grain boundary Josephson junction has been formed. Such steps were observed up to about 65K. Y group superconductors were compared to Bi group superconductors, the relation between manufacturing conditions and characteristics was studied, and practical application of the above device to DC SQUID's was studied. These studies were carried out based on experiments. The results will be reported the day of the meeting.

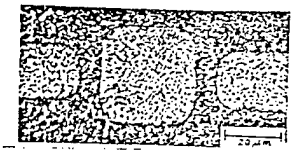
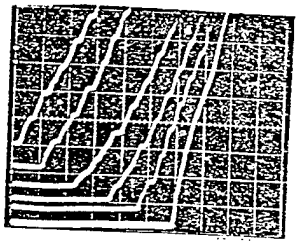


Figure 1. Pattern of Device Prepared (YBCO)



X = 500 μA/div Y = 20 μV/div

Figure 2. Microwave Characteristics (4.2K)

Microbridge Josephson Junction

43067071 Tokyo THE 49TH AUTUMN MEETING OF THE JAPAN SOCIETY OF APPLIED PHYSICS (ABSTRACTS) No 1 in Japanese 4-7 Oct 88 p 149

[Article by Katsuhiko Shinjo, Takayuki Yagi, Atsuko Tanaka, Kiyozumi Niizuma, Tomoko Motoi and Norio Kaneko, Research Center, Canon Corporation: "Fabrication of Microbridge Josephson Junction Using High Tc Superconducting Thin Films"]

[Text] Preface. The creation of Josephson devices using high-temperature superconductors is important in view of the potential practical applications of such devices. To this end, the satisfactory

establishment of microscopic processing technology play a vital role. We have manufactured a microbridge Josephson junction using a dry etching method. Here we provide an outline of our work.

Process. A YBaCuO thin film was deposited on an MgO (100) substrate at a rate of 8000Å by sputtering and was then annealed at 930° to 950°C. Then the thin film underwent photolithography processing using a negative resist. Thus, microbridges were formed by Ar ion milling. Bridge widths were set at 8, 16, and 32 μm.

Results. Figure 1 shows the resistance-temperature characteristics of the device before and after patterning. The onset temperature did not change as a result of patterning, but the end point changed according to bridge width. Figure 2 shows the I-V characteristics of the device at 4.2 K and during its irradiation by 70GHz millimeter waves. During the irradiation by millimeter waves, 10 orders of (Shapiro) steps were confirmed. The characteristics of planar-type and VTB-type devices are being compared. Also, differences in the characteristics of microbridge Josephson junctions using Y group superconducting thin films and those using Bi group superconducting thin films are being studied.

Acknowledgments. We wish to express our appreciation for the great assistance rendered by Professor Kawamura and Assistant Professor Yoshimori of the Tokyo University of Engineering in evaluating the millimeter wave response characteristics in our experiments.

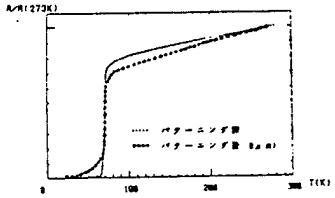
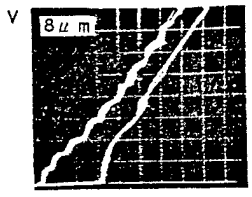


Figure 1.



X Axis: 200 μV/div
Y Axis: 200 μA/div

Figure 2

YBCO Ceramic Device

43067071 Tokyo THE 49TH AUTUMN MEETING OF THE JAPAN SOCIETY OF APPLIED PHYSICS (ABSTRACTS) No 1 in Japanese 4-7 Oct 88 p 149

[Article by Takaaki Ikemachi, Minoru Takai, Teruhiko Ienaga, Toshiaki Yokoo, Yoshinobu Yoshisato, Shoichi Nakano and Yukinori Kuwano, Functional Materials Research Center, SANYO Electric Co., Ltd.: "Characteristics of Superconducting Device Using YBCO Ceramics Prepared by Coprecipitation Method"]

[Text] Preface. Bulk YBCO group superconductors prepared by coprecipitation are composed of microscopic particles (0.5 μm or smaller) as previously reported. The way in which the Jc is affected by a magnetic field differs from that in the general powder method. To investigate the bonding state between particles, the effect of temperature on the Jc was measured. Further, by carrying out bridge processing, the characteristics of bridge responses to electromagnetic waves, light, etc. were investigated, and practical application to devices was studied. An outline of this study is reported below.

Testing method. Samples were prepared by the method previously reported. Then, each sample was processed into a bridge with a thickness of 30 μm and a width of 100 μm (Figure 1) and was used for measurements. Tc ≒ 90K. Jc = 220A/cm^2 (77K).

Results/studies. A maximum Jc of 1300 A/cm^2 (77K) was obtained. The relationship between Jc and temperature in the vicinity of Tc followed the pattern shown in Figure 2. It appears that the structure of the boundary between microscopic particles is close to S-N-S. Further, the bridge proved responsive to microwaves and also to light (Figure 3). We learned that there is a correlation between sample characteristics and the size of the microscopic particles composing each sample and the particle bonding condition. Changes in the Jc produced by the temperatures arising from the heat treatment conditions and the characteristics necessary for the practical application of the samples to devices are described in detail.

Figure 1. Bridge Processing

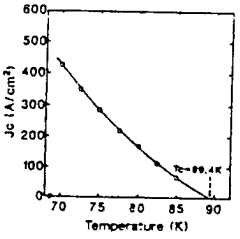


Figure 2. Relationship Between Jc and Temperature

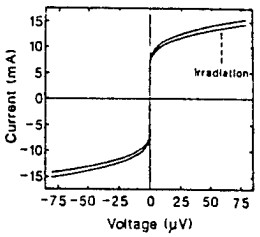


Figure 3. I-V Characteristics During Irradiation by Light

Grain Boundary Josephson Junction

43067071 Tokyo THE 49TH AUTUMN MEETING OF THE JAPAN SOCIETY OF APPLIED PHYSICS (ABSTRACTS) No 1 in Japanese 4-7 Oct 88 p 149

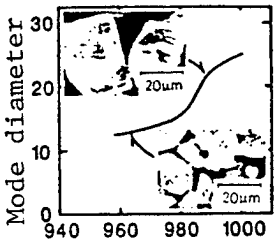
[Article by Maruo Kamino, Kiroshi Suzuki, Toshiaki Yokoo, Yoshinobu Yoshisato, Shoichi Nakano and Yukinori Kuwano, Functional Materials Research Center, SANYO Electric Co., Ltd.: "Grain Boundary Josephson Junction Device Prepared by Plasma-Arc Melting and Rapid Quenching Method"]

[Text] Preface. We have already reported the plasma-arc melting and rapid quenching method, which makes it possible to obtain highly elaborated oxide superconductors.[1] This method can be used to produce amorphous phases in large quantities, making it possible to achieve grain control depending on post-heat treatment conditions. We prepared microbridge devices and studied the relation between grains and grain boundary Josephson effects.

Experiments. Oxide materials (Yb_2O_3, CuO, $BaCO_3$) were blended at a specified rate, formed, plasma-arc melted, and rapidly quenched. Then the oxide materials thus formed were heat treated in oxygen at 920° to 1,000°C for 3 hours. Thus, nearly uniform and highly dense (100%) specimens were obtained. The superconductor particle diameter was measured by optical microscope observation. Further, the specimens were crushed and the particle diameter was measured with a centrifugal sedimentation particle size distribution meter and by SEM. I-V characteristics were measured by the four terminal method.

Results. Figure 1 shows particle diameter at each heat treatment temperature and an SEM image of the specimen. The particle size was about 10 μm in the vicinity of 960°C but grew to about 25 μm at 1000°C. Aeolotropy in the configuration was not observed. The specimen heat treated at 1000°C was processed into a bridge (section: 40 μm X 40 μm) and I-V characteristics under microwave irradiation were measured. The (Shapiro) step peculiar to Josephson junctions was

observed at Ic = 95 μA. This indicates that specimens prepared by the plasma-arc melting and rapid quenching method possess grain boundary Josephson junctions.



Heat treatment temperature. (°C)

Figure 1. Relationship Between Heat Treatment Temperature and Mode Diameter Shown in SEM Image

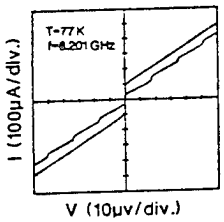


Figure 2. I-V Characteristics Under Microwave Irradiation

Reference

1. 35th Applied Physical Society Meeting preliminary draft 30 aX7

High-Tc Electronic Devices

43067071 Tokyo THE 49TH AUTUMN MEETING OF THE JAPAN SOCIETY OF APPLIED PHYSICS (ABSTRACTS) No 1 in Japanese 4-7 Oct 88 p 151

[Article by Akira Yoshida, Hirotaka Tamura, Norio Fujimaki and Shinya Hasuo, Fujitsu Labs. Ltd.: "Selective Plasma Oxidation for Fabricating High-Tc Electronic Devices"]

[Text] Preface. It it is possible to change high-temperature superconductor carrier density according to places by using a doping or some other method, various potential barriers can be formed against carriers, thus making it possible to manufacture devices as required. We tried to prepare devices by changing the amount of oxygen in Ba-Y-Cu-O thin films using the plasma oxidation method. Here we report an outline of the project.

Results of experiments. A Ba-Y-Cu-O thin film with a thickness of 460 nm was obtained by heat treating multilayer films (prepared by vacuum evaporation) in oxygen. The amount of oxygen contained in the film was reduced by heat treating the film in nitrogen for 1 hour at 600°C. As a result of the deoxidation, the thin film displayed semiconductor-like resistance-temperature characteristics. Through the selective plasma oxidation of the deoxidized thin film, a superconducting region was

created in the semiconductor-like region. A metal mask was used for the selective oxidation process. Figure 1 shows the structure of an experimental device. In the deoxidized region, both superconducting source and drain regions were provided. Thus, a planar-type SNS diode was prepared. Figure 2 shows the I-V characteristics of the diode at 4.2K. It appears that the nonlinear characteristics (observed in the I-V characteristics) were formed by the portion where the superconducting region comes into contact with the nonsuperconducting region.

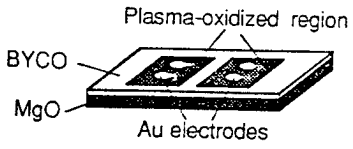


Figure 1. Device Structure

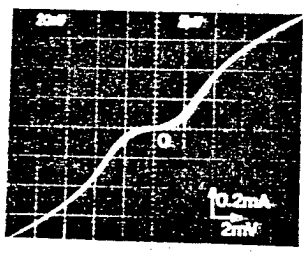


Figure 2. I-V Device Characteristics

Quasi-Particle Injection Device

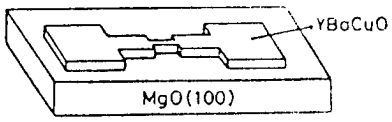
43067071 Tokyo THE 49TH AUTUMN MEETING OF THE JAPAN SOCIETY OF APPLIED PHYSICS (ABSTRACTS) No 1 in Japanese 4-7 Oct 88 p 151

[Article by Koichi Hashimoto, Uki Kabasawa, Masakichi Tonouchi and Takeshi Kobayashi, Osaka University: "High Tc Superconducting 3-Terminal Quasi-Particle Injection Device (II)"]

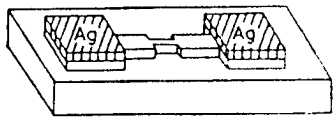
[Text] Preface. It is expected that high-temperature oxide superconductors will play a major role in future electronic devices. Therefore, the study of quasi-particle devices that use high-temperature oxide superconductors is considered to be very important. In our previous report, we described nonequilibrium 3-terminal quasi-particle injection devices that use polycrystalline films. Further, we prepared devices using epitaxial thin films (1600 Å) on an experimental basis and confirmed the operation of these devices. Our report outlines the results of our study.

Experiments. Patterning was carried out, by phosphoric acid etching,[1] on an epitaxial high-temperature superconducting film (YBaCuO) that had been prepared by sputtering. Silver was deposited by vacuum evaporation on this film to form source and drain electrodes. Subsequently, an aluminium electrode was formed to serve as a current injection electrode. Thus, we manufactured an experimental high Tc superconducting 3-terminal quasi-particle injection device (Figure 1).

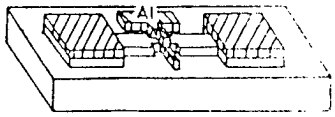
Results. Figure 2 shows the Ic changes when the injection current (Ig) was changed. This figure confirms that the device we manufactured operates as a 3-terminal device. The change in the Ic differed from that of a device made of polycrystalline films. The reason for this appears to be that in the case of polycrystalline film devices,Josephson currents are modulated, while in the case of epitaxial film devices, superconducting critical currents are modulated.



1. Patterning (phosphoric acid etching)



2. Vacuum evaporation of Ag electrode (500°C), 4th annealed)



3. Vacuum evaporation of A1 gate

Figure 1. Device Manufacturing Process

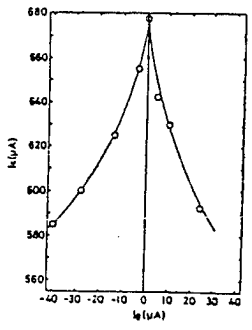


Figure 2. Ic-Ig Characteristics

Reference

1. Y. Yoshizako, M. Tonouchi and T. Kobayashi: Jpn. J. Appl. Phys. 26 (1987)

3-Terminal Device Mechanism

43067071 Tokyo THE 49TH AUTUMN MEETING OF THE JAPAN SOCIETY OF APPLIED PHYSICS (ABSTRACTS) No 1 in Japanese 4-7 Oct 88 p 151

[Article by Uki Kabasawa, Koichi Hashimoto, Masakichi Tonouchi and Takeshi Kobayashi, Osaka University: "Mechanism of High Tc Superconducting 3-Terminal Device"]

[Text] Preface. It is very important to prepare 3-terminal quasi-particle injection devices using high-temperature oxide superconductors in order to investigate not only practical applications but also the physical properties of oxide superconductors. We prepared a 3-terminal quasi-particle injection device and studied its operation using conventional nonequilibrium theory.

Preparation of device. Patterning was carried out, by phosphoric acid etching, on a high-temperature superconducting film (YBaCuO) prepared by sputtering. Silver was deposited by vacuum evaporation on this film to form source and drain electrodes, and an aluminium electrode was formed to serve as a current injection electrode. Thus, we prepared a 3-terminal device (Figure 1).

Results and studies. Figure 2 shows the relationship between the injection current (Ig) and the intersource/drain critical current (Ic). The solid line is a curve based on the Owen-Scalapino theory of nonequilibrium.[1] This curve reproduces the pattern of experimental data. This pattern suggests that a nonequilibrium phenomenon similar to the conventional nonequilibrium phenomena occurs in the recently manufactured oxide superconductors.

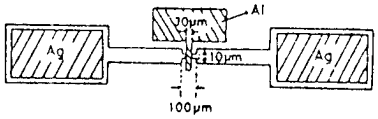


Figure 1. 3-Terminal Device

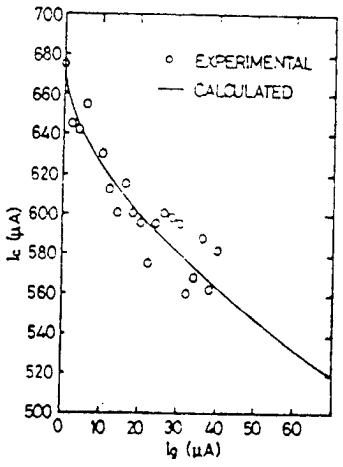


Figure 2. Ic-Ig Characteristics

Reference

1. C. S. Owen and D. J. Scalapino, Pys. Rev. Rett. 28, 1559 (1972)

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